The invention relates to a phase discriminator for producing an output voltage which is dependent upon the phase difference between a first and a second pulse train. Such a phase discriminator is required, for example, in the PLL circuit to produce the clock signal or the so-called bit timing from a bit string which represents a digital signal, e.g. a PCM signal in the transmission code.

At the output of a transmission arrangement for digital signals (e.g. a digital recording device) there is almost always the problem of retrieving the clock signal or the bit timing of the incoming bit string. This usually takes place with the aid of a PLL circuit. The type of phase discriminator used in the PLL circuit can have a strong influence on the properties of the PLL circuit. There are also endeavours to construct the PLL circuit within a digital signal processing circuit as far as possible from digital basic elements, i.e. gates and flipflops. A phase discriminator for digital signals which merely consists of an ex-OR gate is set out in EP-A-0 009 939.

The said known circuit, the disadvantage which occurs with it and the considerations and knowledge on which the invention is based are explained below with the aid of Figures 1 to 3. In this case Figure 3a shows the characteristic of a known phase discriminator and Figure 3c shows the modified characteristic of a phase discriminator constructed according to the invention.

A PLL circuit with the known phase discriminator is shown in Figure 1. Figure 2 shows the appertaining signal patterns. From each change of level of the incoming bit string A a pulse having the pulse width τ is produced by the delay element 4 with the delay time τ and the ex-OR gate 5, where τ should be as nearly equal to half the bit duration T as possible. The first pulse train B produced in this way as well as the second pulse train which is produced in the oscillator 1 and is here equal to the bit timing C are delivered to the two inputs of the ex-OR gate 2 which serves as the phase discriminator. The output signal B $\oplus$ C of the gate 2 produces the control voltage UR for the oscillator 1 behind the low-pass filter 3 which serves as the loop filter. The discriminator characteristic, i.e. the course of the control voltage UR over the phase φ between B and C, is shown in Figure 3a. The working point of the PLL circuit is set for example by adjustment of the oscillator 1 to $\varphi = 90°$.

For this setting a distribution curve for the position of the changes of level of the bit string A is given in Figure 3b. The changes of level concentrate here for example on the range 90° +- 30°. The scattering of the changes of level results from time jitters, that is to say time errors, of a playback device, signal distortions and back-

ground noise. So long as the bit timing C follows the time jitter of the bit string A, the time jitter does not contribute to widening of the distribution curve in Figure 3b. A widening of the distribution curve means that the probability of bit errors occurring is increased. Therefore the bit timing C should follow the time jitter as closely as possible. For this purpose the discriminator curve must have a specific minimum slope in its main working area. Consideration of Figures 3a and 3b will reveal that the discriminator curve also rises further in terms of magnitude outside its main region, which here lies at 90° +- 30°. As a result changes of level which occur rarely are of particular importance for the generation of the control voltage, although these changes of level are probably not relevant for setting the correct timing phase. Since the statistically rare changes of level occur in large numbers in the case of breaks in the level, this phase discriminator is not ideally suited for undisrupted timing regeneration. When changes of level occur in large numbers outside the main scatter area the timing phase can be falsified particularly severely, and the probability of bit slips occurring is increased.

The object of the invention is to construct a phase discriminator in such a way that the control voltage which is generated is not falsified to a great extent by phase differences between the bit string and the bit timing which deviate greatly from the basic value. It should also achieve a way of producing the phase discriminator largely from digital basic components.

This object is achieved by the invention described in claim 1. Advantageous further embodiments of the invention are described in the subordinate claims.

The expression "phase density distribution" is one which is known *per se*. It means the representation of the frequency with which the respective phase difference between the bit string and the bit timing produced therefrom occurs in the case of a large number of changes of level, in the form of a distribution curve. In a bit string which is free from time errors, this distribution curve has a basic value, e.g. 90°, which is set by the oscillator of the PLL circuit. When the bit string has no time errors and also no other disturbances are present, the phase difference in all comparison operations between the bit string and the bit timing has this same basic value. The distribution curve would then be only a vertical dash in this basic phase. As a result of unavoidable time errors in the bit string there are deviations from this basic phase which can be represented in the form of a distribution curve. What the invention now achieves is that, in the case of phase differences which deviate widely from the said basic value and therefore with a high degree of probability do not

represent a measure for the actual phase difference, the discriminator characteristic has a very flat course, whilst the characteristic in the region of the least disturbed changes of level has the greatest slope. In a known phase discriminator, with a greater phase difference according to a preferably linear characteristic a correspondingly large control voltage is also produced. However, this is not desirable in the present case because such great phase differences are generally not representative for the signal and would effect an undesirable alteration of the control voltage produced, particularly when severe phase deviations occur in large numbers in the case of specific signal disturbances, e.g. dropouts.

The invention will be explained below with the aid of Figures 3c to 6, in which:

Figure 3c shows the modified characteristic of the phase discriminator achieved by the invention,

Figure 4 shows a circuit for carrying out the invention,

Figure 5 shows curves for explanation of the way in which the circuit according to Figure 4 functions and

Figure 6 shows a circuit according to one embodiment of the invention.

Figure 3c shows a discriminator characteristic in which the inclination corresponds to the phase density distribution represented in Figure 3b. This discriminator characteristic can be produced not only by the limitation of a discriminator characteristic according to Figure 3a, for example up to the broken line. Above all it should be taken into consideration that the width of the distribution curve can alter according to the quality of the signal transmission. The sloped region of the discriminator curve must then be adapted automatically to the phase density distribution. A phase discriminator circuit which effects this is shown in Figure 4. The appertaining signal patterns are shown in Figure 5. The pulse train B obtained from the modulated bit string A again represents pulses of constant duration τ which mark the time position of the changes of level of the bit string A. The duration τ does not have have to be equal to half of the bit duration T. It should merely be smaller than the smallest level change distance of the bit string A. The pulse duration τ actually acts on the amplitude of the output voltage UR.

In the phase discriminator according to Figure 4 the D-type flipflop 6 establishes whether a change of level of the bit string A occurs before or after a falling edge of the bit timing pulse C. The delay element 7 with the delay $\tau 1$ serves for equalisation of the running time of the D-type

flipflop 6. Depending upon the output voltage Q of the D-type flipflop 6 a negative pulse E then appears at the output of the NAND gate 8 or a positive pulse F at the output of the AND gate 9. After addition of the pulses E and F in the addition stage 10 and low-pass filtering in the low-pass filter 11 the voltage UR' is obtained, the course of which is shown in the discriminator characteristic in Figure 3c. The slope of this characteristic corresponds to the phase density distribution of the changes of level of the bit string A. This effect comes about because each change of level of the bit string A has the same importance in terms of magnitude for generation of the voltage UR. In the phase discriminator in Figure 1 this importance was dependent upon the phase deviation of the respective change of level.

However, if each pulse in the pulse train B has the same importance for the voltage generation, then the inclination of the voltage curve UR at a specific phase deviation φ must correspond to the frequency of the pulses in the pulse train B with the relevant phase position. This relationship can also be represented in the following way: Each value UR (φ) corresponds to the integral of the entire phase density distribution curve, so that the part of the distribution curve lying behind the deciding edge of the bit timing pulse C is reflected on the abscissa. The disadvantage that changes of level with a large phase deviation, which it is highly probable are not relevant for the generation of the control voltage in a PLL, act with greater emphasis on the control voltage generation is eliminated here.

By the combination of the pulses E and F in the addition stage 10 and the subsequent integrating low-pass filter 3, the output voltage UR corresponds to the condition of a counter which counts forwards with one pulse train and backwards with the other pulse train. Therefore the phase discriminator shown in Figure 4 may be designated as a counter/phase discriminator.

Figure 6 shows advantageous embodiments of the described phase discriminator within a regeneration circuit for a transmitted bit string A. The outputs of the circuit supply the regenerated bit timing C and the bit string A' keyed with this bit timing. In the phase discriminator shown in Figure 6, by contrast with the basic circuit shown in Figure 4, several details are given as an example of the embodiment. The addition stage 10 which is formed by two resistances 12, 13 and the subsequent low-pass filter 3 which serves as a loop filter are combined into the RC combination which is shown between the outputs E and F and the non-inverting input of an OP amplifier 14. The control amplification can be set to the desired value with the OP amplifier 14. The centre frequency of the PLL circuit is

determined by the basic voltage Uo applied to the amplifier circuit.

The delay equalisation $\tau 1$ by means of the delay element 7 for the D-type flipflop 6 in Figure 4 is formed in Figure 6 by a similar D-type flipflop 15 which transmits the B pulses. The transmission can be prevented by applying the voltage "0" to the D input of the flipflop 15. This may be sensible in the case of a break in the level of a digital signal scanned by a recording device, and certainly when the level falls so low that the changes of level of the bit string A predominantly represent amplified background noise.

It may be regarded as a further advantage of the phase discriminator according to Figure 4 or 5 that the pulses for the changes of level of the bit string A occurring before and after the deciding flank of the bit timing pulse C are available at separate outputs E and F. This makes it possible in a simple manner to carry out automatic optimisation of the timing phase for the scanning of the bit string A. As a result a circuit adjustment is not necessary. The bit error rate is automatically kept to a minimum value, and in the event of disconnection of the synchronising pulses B during a break in the level the phase only drifts minimally because of the continuously optimised centre frequency of the oscillator 1, so that the probability of bit slips occurring is reduced.

In Figure 6 the automatic optimisation of the scanning phase is carried out with the aid of a forwards/backwards counter 16 and a D/A converter 17. The pulse voltages E and F are delivered to the two inputs of the forwards/backwards counter 16, possibly via additional frequency dividers 18, 19. In order to be able to achieve a good averaging in the comparison of the pulse counts of E and F, the divider ratios n and m of the additional frequency dividers 18, 19 and the step number of the forwards/backwards counter 16 are comparatively high. The peak-value outputs of the forwards/backwards counter 16 are delivered to the D/A converter 17. The output voltage of the D/A converter 17 forms the basic voltage Uo for setting the centre frequency of the oscillator 1. The oscillator 1 should only be influenced by the voltage Uo in very small steps. As the formulae in Figure 6 show, this can be carried out for example by the choice of a correspondingly small resistance R between the output and the inverting input of the operational amplifier 14. With the correct polarity of the voltage Uo the PLL circuit is then automatically set so that the equation $E : F = m : n$ is met, where E and F represent the pulse counts at the relevant outputs. Normally m will equal n. Also, one of the values m, n or both values can be "1", i.e. the corresponding divider is omitted.

With a symmetrical distribution curve as in Figure 3b, the case m = n will produce the minimum bit error rate. This may be explained as follows: It is known that the quality of a transmitted bit string can be assessed with the aid of the so-called eye diagram. The eye diagram is obtained by representing the bit string on an oscillograph triggered by the bit timing pulse C. The eye diagram shows accumulations of changes of level spaced from the bit duration T. The more concentrated these accumulations are, i.e. the fewer changes of level occur between the accumulations, the more the bit string can be regenerated without errors, provided that the scanning necessary for the regeneration takes place at the greatest distance from the accumulation points. The level change density of the eye diagram can be represented by a periodic repetition of the distribution curve of Figure 3b spaced from the bit duration T. If for the timing regeneration in the PLL circuit automatic means ensure that one edge of the bit timing pulse C is always set to the centre of the level change accumulations, then with a symmetrical timing voltage the other edge of the pulse is the maximum distance from these accumulations. Thus, so long as this edge is used for the regenerating signal scanning, the minimum error rate is produced.

According to Figure 5 the phase control is achieved with the aid of the falling edge of the bit timing pulse C. The scanning of the transmitted bit string A is carried out with the aid of a positively edge-triggered D-type flipflop 20, i.e. with the rising edge of the bit timing pulse C. The scanning instant is automatically placed at the time of lowest level change frequency.

In Figure 6 the possibility of switching off the pulses at the outputs E and F in the case of breaks in the level or in transmission intervals ensures that during these periods the centre frequency of the PLL is maintained. So that the oscillator of the PLL also oscillates immediately at the correct frequency after switching on, the input values for the D/A converter 17 can be stored in a non-volatile store. A corresponding additional register, for example, serves for this purpose, or the current supply of the output flipflop of the forwards/backwards counter is maintained with the aid of a battery when the device is switched off, so that its state remains unchanged until reconnection occurs.

The description relates to binary pulse trains. However, the invention is also applicable to multiple-stage transmission codes, e.g. ternary codes.

Claims

1. Phase discriminator for producing an output voltage which is dependent upon the phase difference between a first pulse train (A, B) and a second pulse train (C), particularly for a PLL circuit for producing the bit timing from a PCM signal, characterised in that means are provided which cause each pulse of a first pulse train, according to its phase deviation from a second pulse train or depending upon whether the reference edge of the relevant pulse of the first pulse train falls on the positive or negative half-wave of the second pulse train, to generate a pulse of constant length at one of two outputs, and that the output voltage of the phase discriminator is dependent upon the difference in the pulse counts at the two outputs, the output voltage being formed by combination and integration of the pulses (E, F) at the two outputs and/or by determination of the pulse count difference with the aid of counter circuits (16, 18, 19) and D/A conversion of the counter result.

2. Discriminator as claimed in claim 1, characterised in that the pulse train (B) derived from the first pulse train (A) consists of pulses which mark the time position of the changes of level of a bit string (A), and that the second pulse train is a bit timing pulse (C) with equidistant level changes, that each pulse of the pulse train (B) derived from the first pulse train (A) influences the output voltage (UR) in terms of magnitude in the same way, whilst the influence in terms of direction is dependent upon whether the reference edge of the relevant pulse falls on a positive or negative half-wave of the second pulse train (C).

3. Discriminator as claimed in claim 1 or 2, characterised in that the pulses of the pulse train (B) derived from the first pulse train (A) are switched off as soon as the probability exists that these pulses are produced predominantly by spurious signals.

4. Discriminator as claimed in one or more of claims 1 to 3, characterised in that the pulses of the pulse train (B) derived from the first pulse train (A) are counted with a forwards/backwards counter (16), the direction in which it counts being dependent upon whether the pulses fall on the positive or negative half-wave of the second pulse train (C), and the counter result is converted with the aid of a D/A converter (17) into a voltage (Uo) which serves as a supplement to the output voltage (VR).

5. Discriminator as claimed in claim 4, characterised in that the forwards/backwards counter (16) has separate counter inputs, and frequency dividers (18, 19) are connected upstream of these inputs.

* C L M S *

6. Discriminator as claimed in claim 4 or 5, characterised in that the counter result of the forwards/backwards counter (16) is stored in a non-volatile store.

* C L M S *