

The invention is based on a scanning pattern correction circuit in a television device according to the preamble of claim 1.

Such measures for scanning pattern correction are especially necessary in projection television devices because with these, the three images for R, G, B superimposed on the projection surface are generated by three spatially separated picture tubes, each working with a deflection unit. In this case, the scanning pattern correction generally serves to compensate geometry errors in the pattern described on the projection surface, for example, for compensating north-south or east/west errors, for eliminating non-linearities in the deflection or for achieving the convergence between the three beams for R, G, B.

With such a convergence device, a grid pattern composed of horizontal and vertical lines is formed on the projection surface. Correction values for the convergence of the three colours red, green, blue in the horizontal and vertical direction are determined for the crossing points of the grid pattern. These correction values are stored and serve for successive correction of the convergence at the individual crossing points during scanning of the picture screen. As the correction values are only valid for the crossing points, a respective linear interpolation from one correction value to the next is carried out between two crossing points. It is necessary to fade over from one correction value to the next between two successive crossing points, for example, in the vertical direction.

Such projection devices function, however, in various modes with differing numbers of lines between two crossing points situated above each other vertically. This is the case when a different vertical scanning is being used to present differing picture formats and the number of lines

falling within the effective projection area is different, see e.g. EP-A-0291924.

It is the object of the invention to provide a simple circuit for generating a delta-type voltage for the fade-over between two correction values which adapts, in particular, to differing values of the lines between two crossing points.

This task is solved by the invention specified in claim 1. Further advantageous developments of the invention are specified in the dependent claims.

Through using the circuit operating digitally according to the invention, it is ensured that the maximum value of the delta voltage for the fade-over is always reached following a precisely defined number of lines which corresponds to the number of lines between two successive crossing points. By means of the digital method of functioning, preferably adjusted by means of a processor, tolerances are excluded as far as possible so that the circuit always operates without error, even in the case of differing numbers of lines between two crossing points, and effects an exact linear interpolation. Thus, the circuit always functions faultlessly in various modes, i.e. with differing numbers of lines during the visible picture area, i.e. also differing numbers of lines between two crossing points of the grid pattern.

The invention will be explained by means of the drawing using the example of the convergence correction for a projection television device. There is shown in

Figure 1 the principles of the delta voltage for the fade-over which can be achieved through the invention,
Figure 2 a block circuit diagram of the invention, and
Figure 3 a practical embodiment of the circuit according to Fig. 2.

In Fig. 1 it is assumed that crossing points of the grid pattern have a spacing of five lines in the vertical direction, i.e. the crossing points are located at lines 5, 10, 15, 20, ... Allocated to these lines are convergence correction values K_1, K_2, K_3, K_4 determined with the convergence adjustment and stored in memories which values, as a rule, differ from crossing point to crossing point. Therefore, in each case a linear interpolation from one crossing point to the next crossing point is necessary, i.e. a continual or step-wise fade-over of the effective convergence correction value, for example, from K_1 to K_2 , K_2 to K_3 , etc. This is carried out by the stepped delta voltage x illustrated which effects a change between the correction values K_1, K_2, K_3, K_4 in five steps. This stepped correction voltage x functions like the linear delta voltage x_1 also illustrated.

Fig. 2 shows a circuit for achieving the fade-over from one correction value K to the next. A register 1 supplies a series of equal digital words d ; to be precise, one word d in each of the N lines between two correction values K .

These digital words are fed to the adder 2, the output of which is connected to the input of the register 3. A series of line-frequency impulses H are applied to the register 3 from the terminal 4. The output 5 of register 3 is connected via line 6 to a second input of the adder 2 and also supplies the stepped voltage x in digital form, designated $x(D)$. By feeding back the output value of register 3 to the adder 2 in every line, the stepped signal x according to Fig. 1 arises at output 5 of register 3 and climbs by one step during each line.

After the time T between two successive crossing points and correction values, the decoder circuit 21 detects that $x(D)$ has reached a value of 1. It supplies a signal to the input S of RS flipflop 22. Thereby, flipflop 22 alters its

state and, therewith, the value US at its output which is connected to the control input of adder 2. A reversal in the function of the adder 2 then takes place in the sense that during the next period T , i.e. between $K2$ and $K3$ in Fig. 1, a digital word d is subtracted from the output value of register 3 in the adder 3 so that the value x decreases again step-wise and approximates the delta-type voltage x_1 .

At point $K3$ $x(D)$ again reaches a value of 0. This value is detected by the decoder 20. The RS flipflop 22 is reset via input R so that the value of US is altered and controls adder 2 to the adding state.

The digital signal $x(D)$ from output 5 is fed via line 7 to the D/A converter 8 which thereupon generates an analog voltage $x(A)$. This ideal staircase-type voltage is, in practice, smoothed out by a low-pass filter, i.e. it is approximated to the ideal linear delta form x_1 according to Fig. 1. On the other hand, this voltage arrives as control voltage to the multiplication stage 9 and as the value $(+1-x)$, i.e., in the form indicated by the broken line, to the multiplication stage 10.

The memory 11, in which the convergence correction values are stored, supplies, at the illustrated moment in time, the correction values $K1$, $K2$ via two D/A converters 23, 24 which values arrive at the inputs of the multiplication stages 9, 10. In the multiplication stage 9, the value of $K1$ is linearly reduced by the voltage x during time T from the maximum value of 1 to a value of 0. On the other hand, in multiplication stage 10, the value $K2$ is raised during time T from the value of 0 to the maximum value of 1. The output voltages from the stages 9, 10 are added in the addition stage 12. The correction signal ensuing at output 13 is, therefore, always a linear interpolation between successive correction values $K1$, $K2$, $K3$, $K4$ during a time T . Consequently, the circuit effects a linear fade-over between

two successive correction values for the individual crossing points respectively as is desirable for an optimal correction of the convergence for the lines lying between two crossing points respectively.

Fig. 3 shows a practically tested circuit for the upper section in Fig. 2 with the components 2, 3, 4, 5, 6. The input 14, designated as V-Reset, serves for resetting to zero at the start of every field. The input 15 effects the described switch-over between the counting up and the counting down respectively in adder 2 (up/down) always at a crossing point K. The adder 2 is formed by the four adding stages illustrated with two or four bits respectively. The reversal between the counting up and the counting down through the digital words d each with 10 bits is carried out by the EXOR gates 16, 17, 18 which are reversed by the LSB signal from input 15 at a respective crossing point K. The register 3 functions as in Fig. 2 and supplies, at the input 5, the digital signal $x(D)$ which represents the delta voltage x according to Fig. 1. The register 3 is, as in Fig. 2, controlled by the line-frequency impulses H from terminal 4. For the number N of lines between two crossing points (5 in Fig. 1) on the one hand, and the numerical value of d on the other, there results, in practice, the following values with differing vertical deflection amplitude depending on the mode used:

N	d
64	255
48	341
42	390
40	409
36	455
35	468
30	546
56	292
32	510
24	682

21	780
20	818
18	910

The reversal always at a crossing point K can also be carried out in that at the output of register 3, there is provided a decoder which determines the maximum value of the voltage x and thereupon, triggers the reversal. The highest binary number for the maximum value of the delta voltage x according to Fig. 1 appearing there has a value of, for example, 16383.



Claims

1. A circuit for scanning pattern correction in a television device in which correction values for crossing points defined by a grid pattern and separated by N lines are stored and an interpolation from one correction value to the next takes place between the crossing points by means of a delta voltage, **characterised in that** during each of the N lines, the same digital word (d) is applied to the input of an adder (2), the output of which is connected to an input of a register (3) controlled by line-frequency pulses (H), in that the output of the register (3) is connected to an input of the adder (2) and the input of a D/A converter (8) supplying the delta voltage (x), in that, alternately, in each case from one crossing point (K) to the next, the digital word (d) is added to the output value of the register (3) and from the next to the next-but-one crossing point (K) is subtracted, and in that the correction values (K1, K2) for two crossing points situated vertically one below the other are applied, via two multiplication stages (9, 10), to an adding stage (12) supplying the interpolated values, and the delta voltage (x) is applied to the multiplication stages (9, 10) in the sense of a reversing change of their multiplication factors, and in that at the output (13) a correction signal arising provides a respective linear interpolation during a defined time (t) between two successive correction values (K1, K2, K3, K4).

2. A circuit according to claim 1, **characterised in that** the number (N) of lines is adjustable during which the digital words (d) are fed to the adder (2) and added to or subtracted from the output value (x) of the register (3).

3. A circuit according to claim 1, **characterised in that** EXOR gates (16 - 18) are located prior to the adder (2), the gates being reversed in each case at a crossing point (K) for



switching over the polarity of the digital words (d) (Fig. 3).

4. A circuit according to claim 1, **characterised in that** a decoder (21) is provided which detects the maximum value (16383) and a further decoder (20) which detects the minimum value (0) at the output of the register (5) and in that a switch-over of the adder (2) from addition to subtraction or vice versa is triggered by the decoders.

5. A circuit according to claim 1, **characterised in that** the circuit is used as a convergence arrangement in a projection television device for interpolation of the convergence-correction values (K).