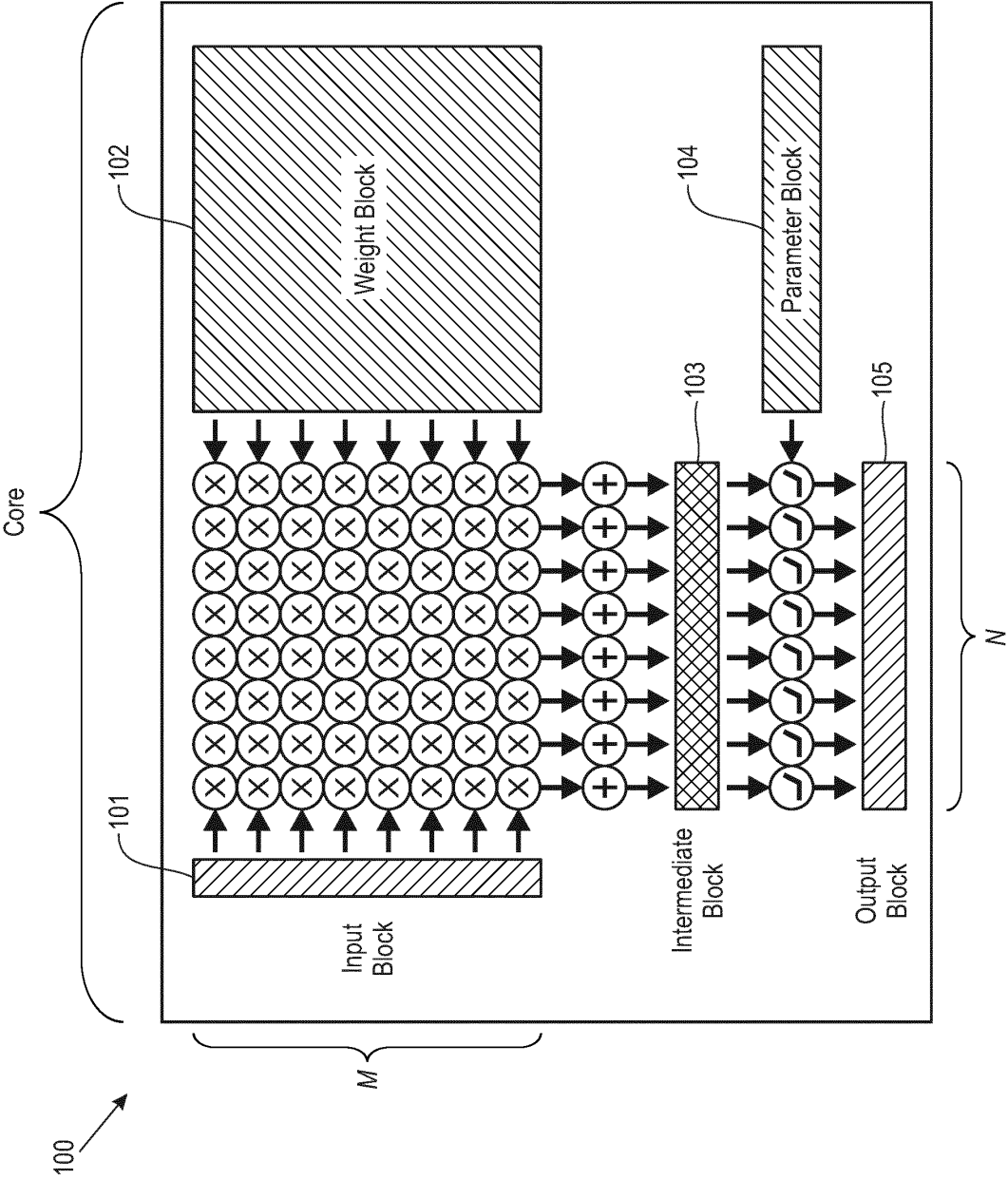




200

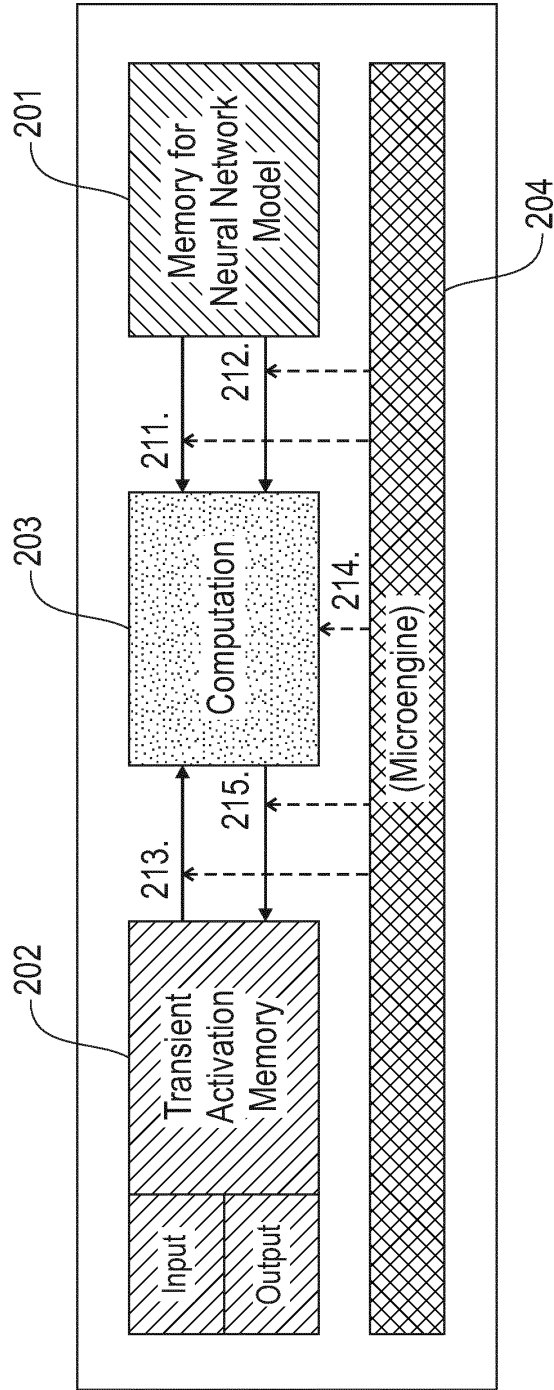


FIG. 2

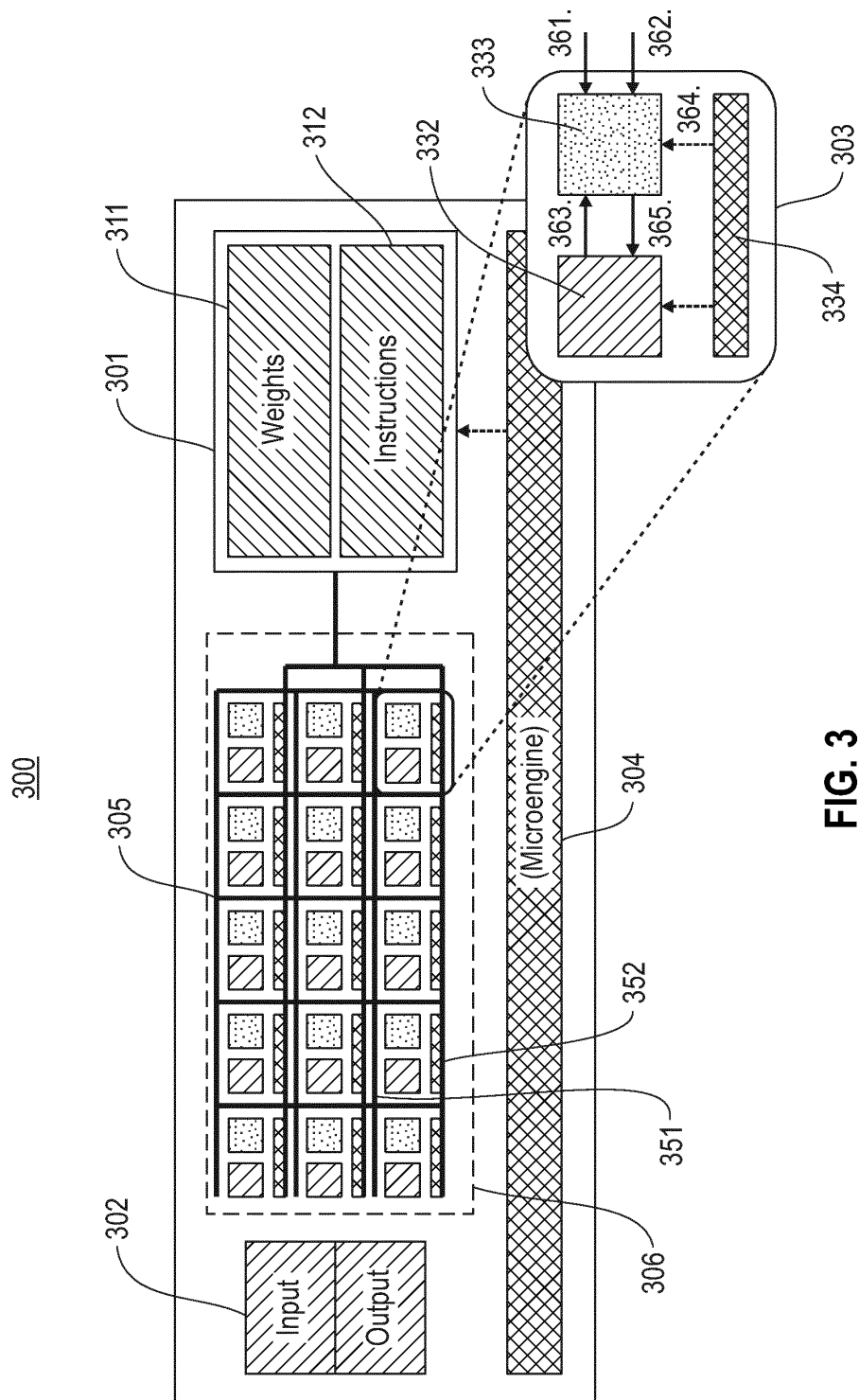


FIG. 3

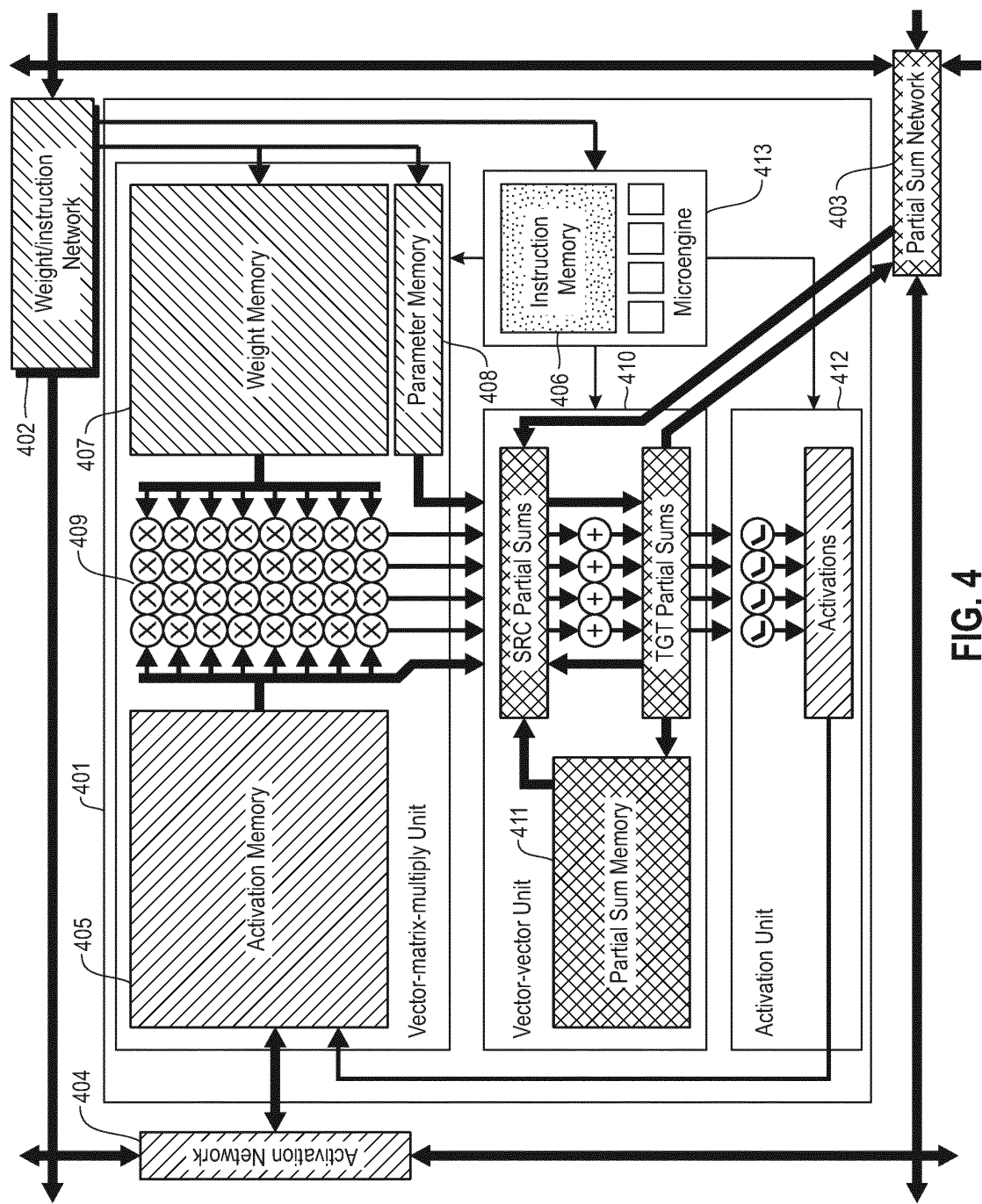


FIG. 4

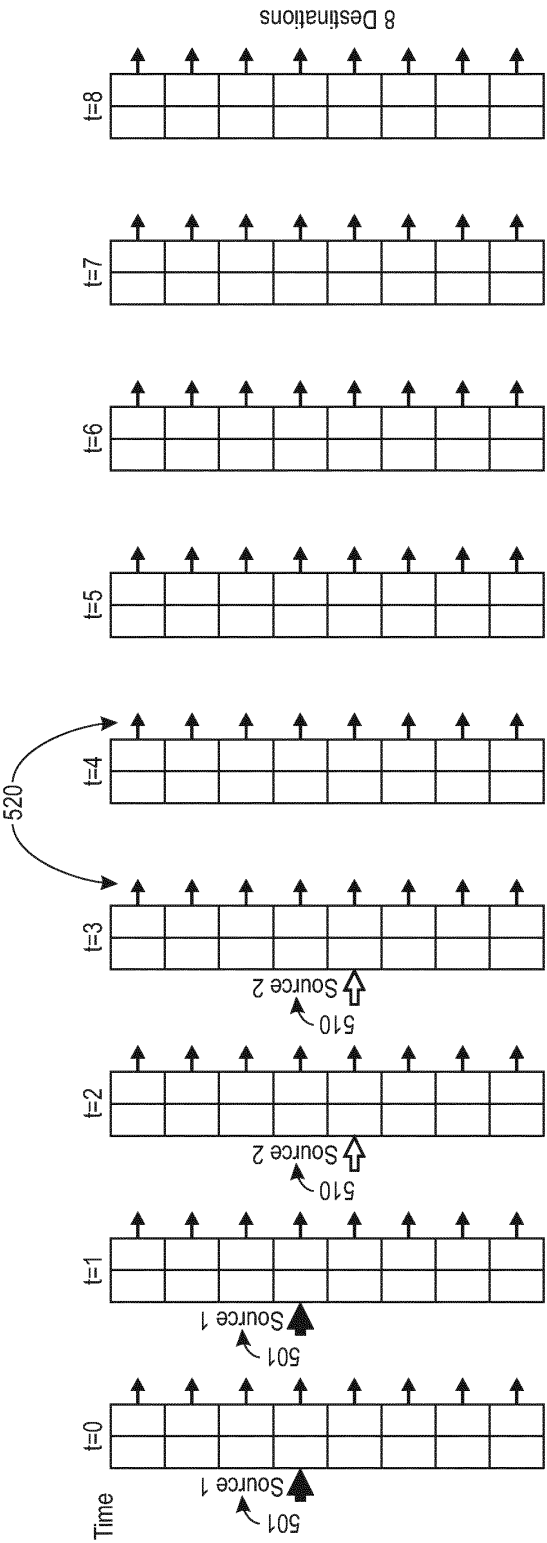


FIG. 5

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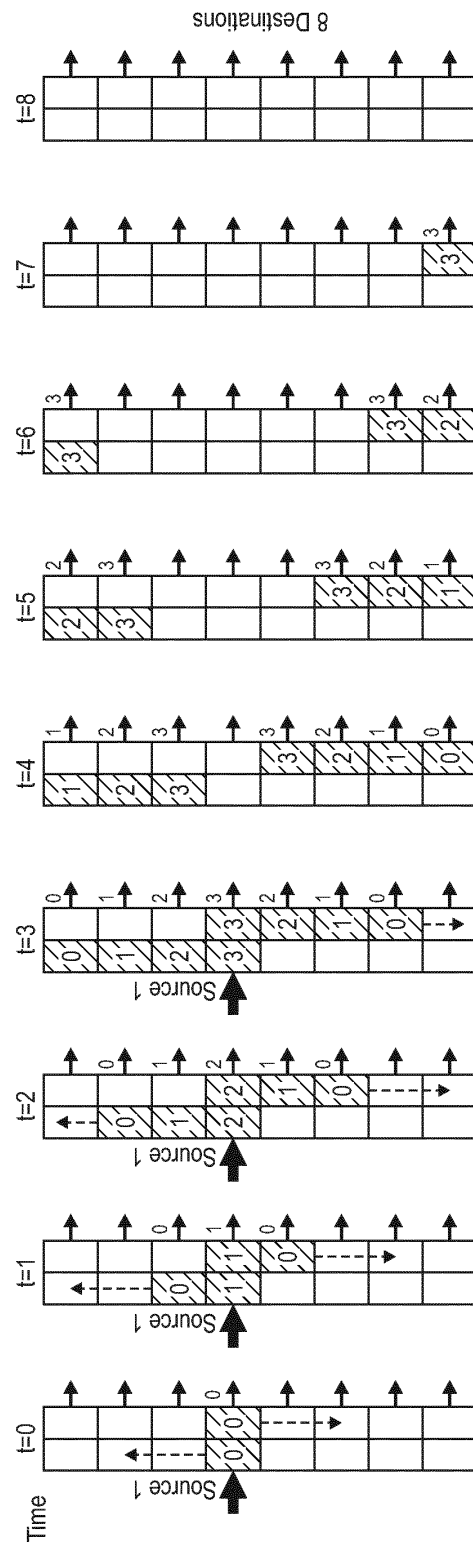


FIG. 6

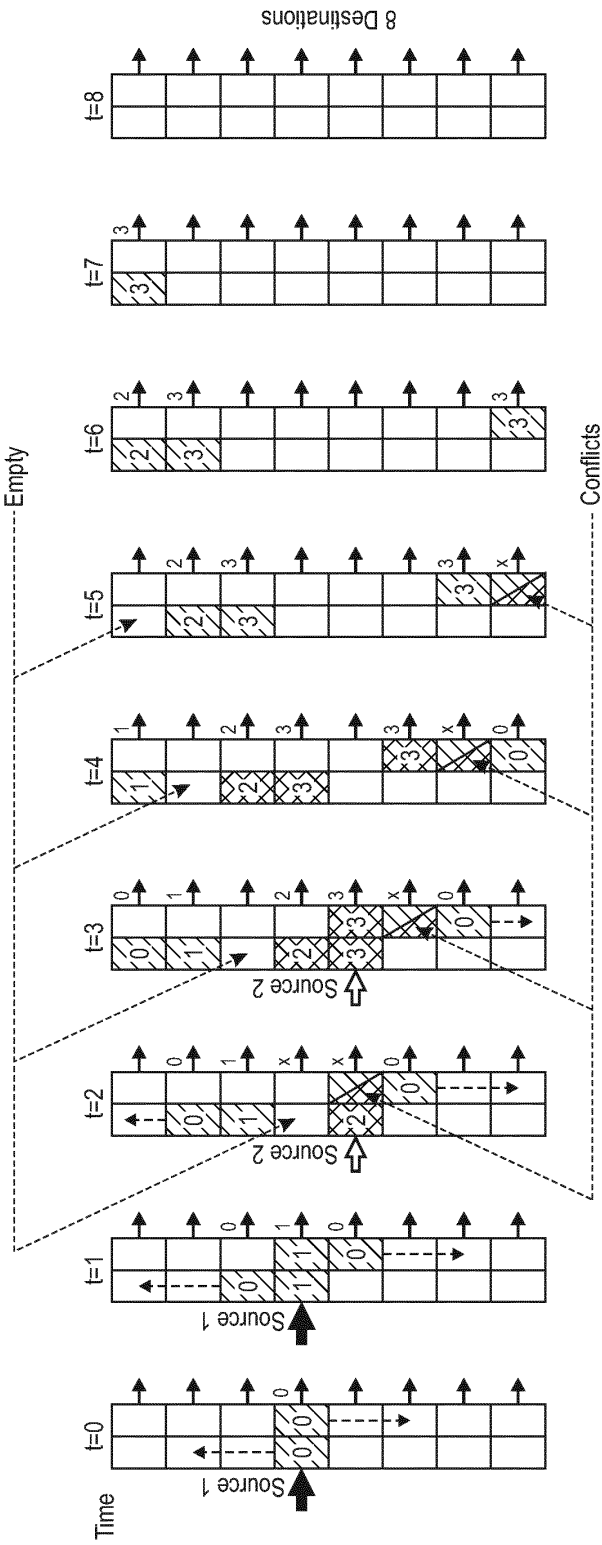


FIG. 7

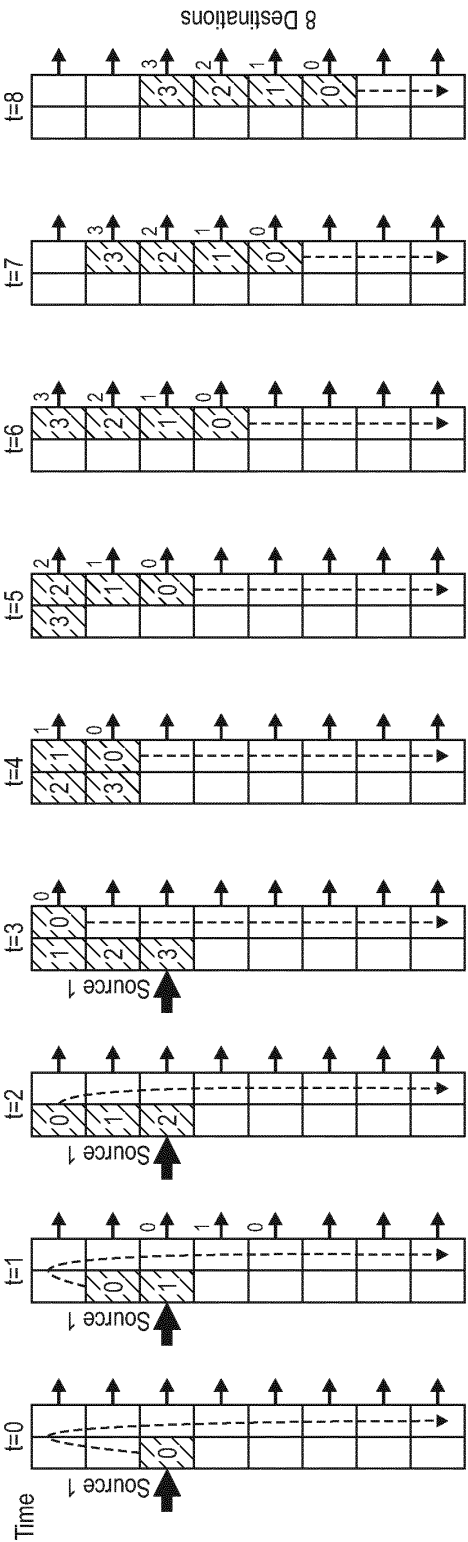


FIG. 8

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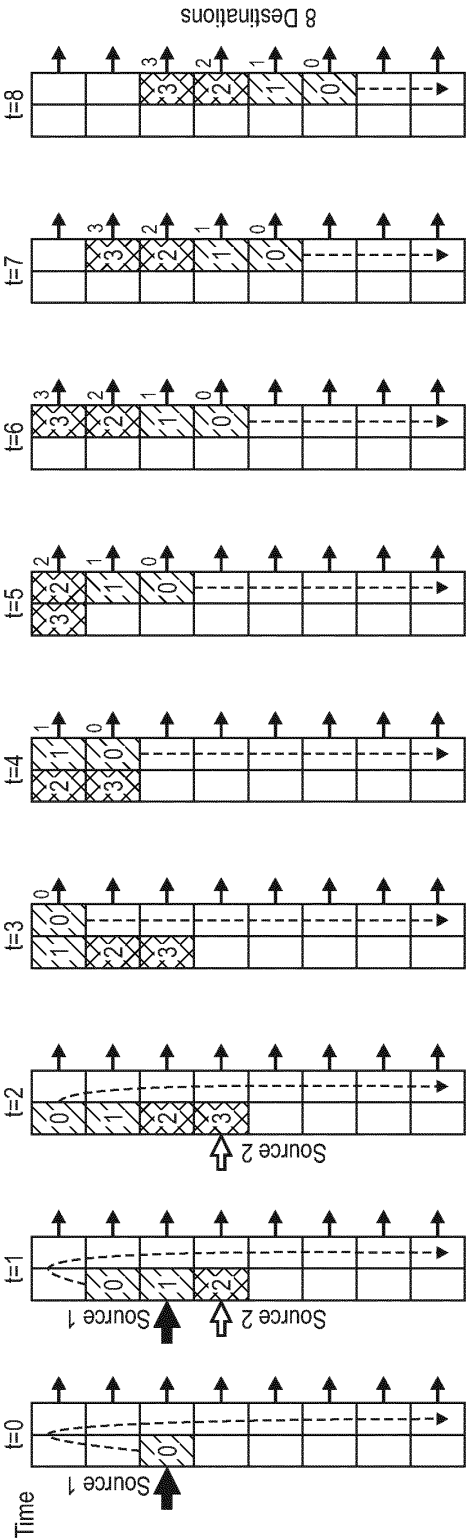


FIG. 9

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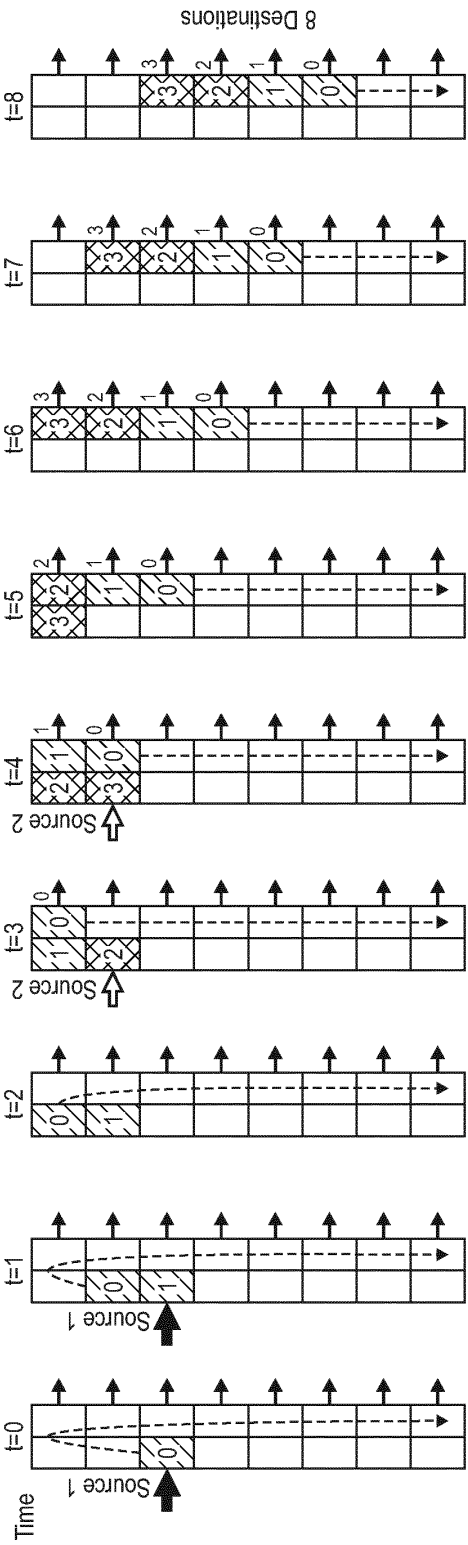


FIG. 10

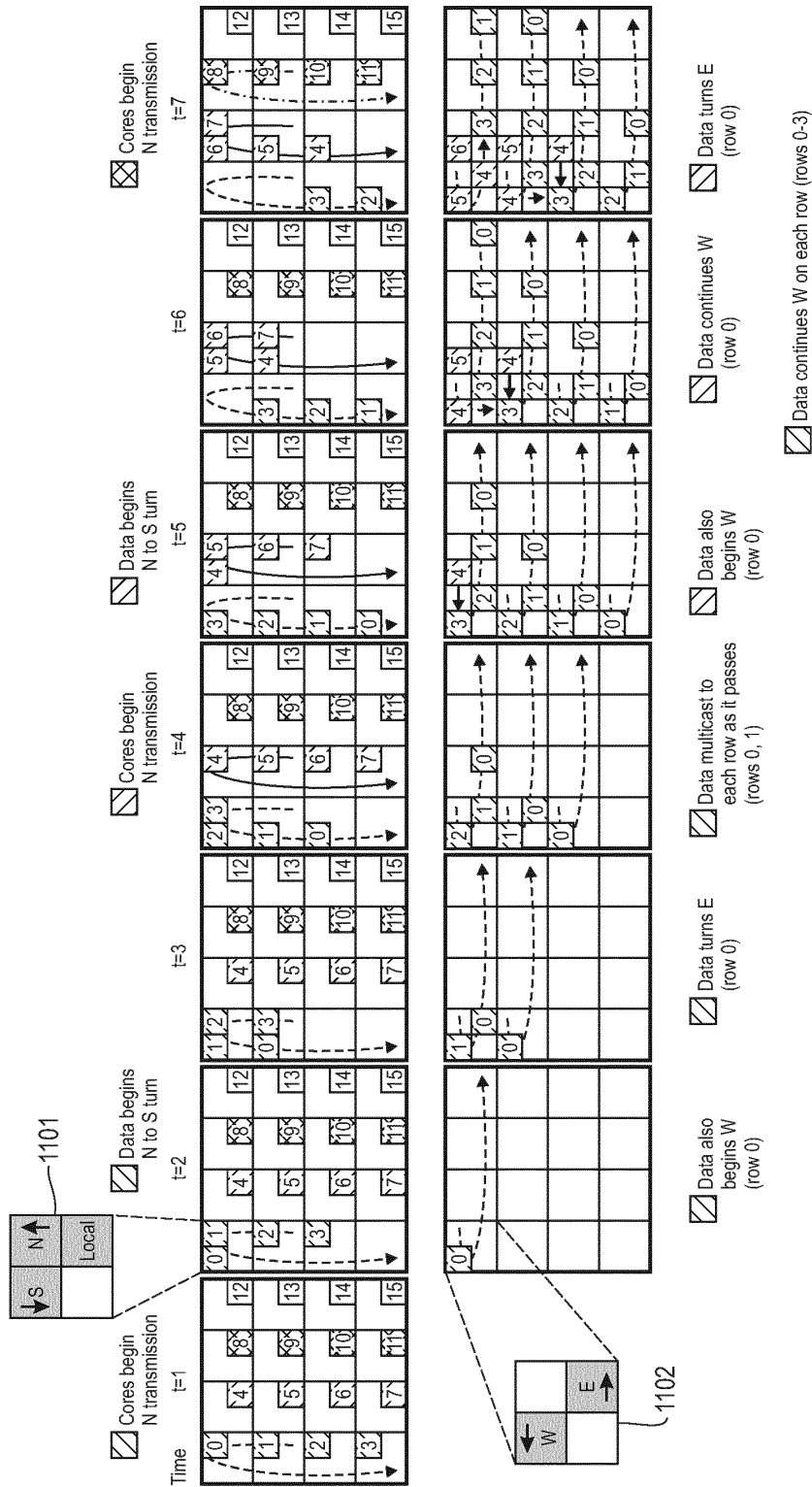


FIG. 11

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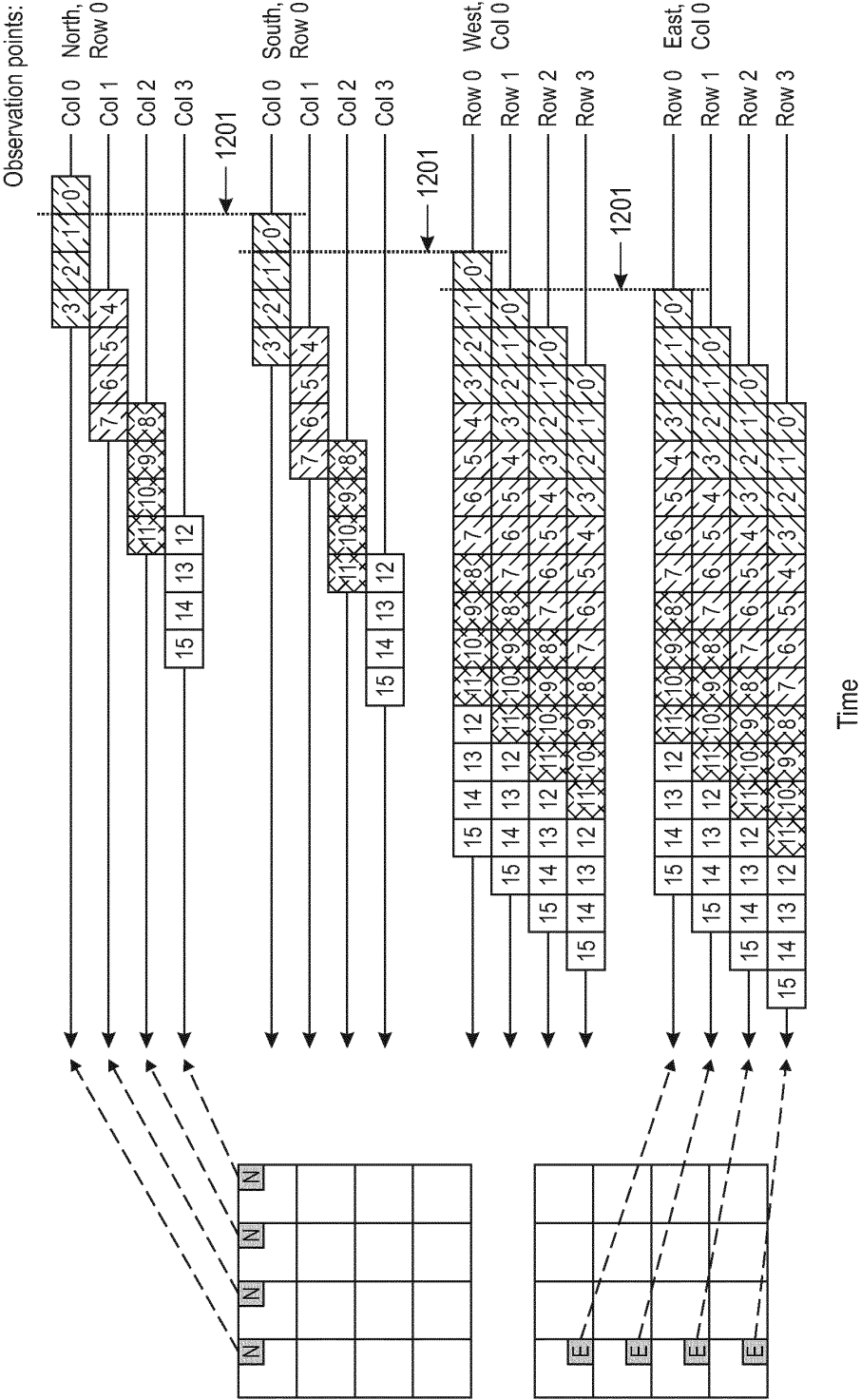


FIG. 12

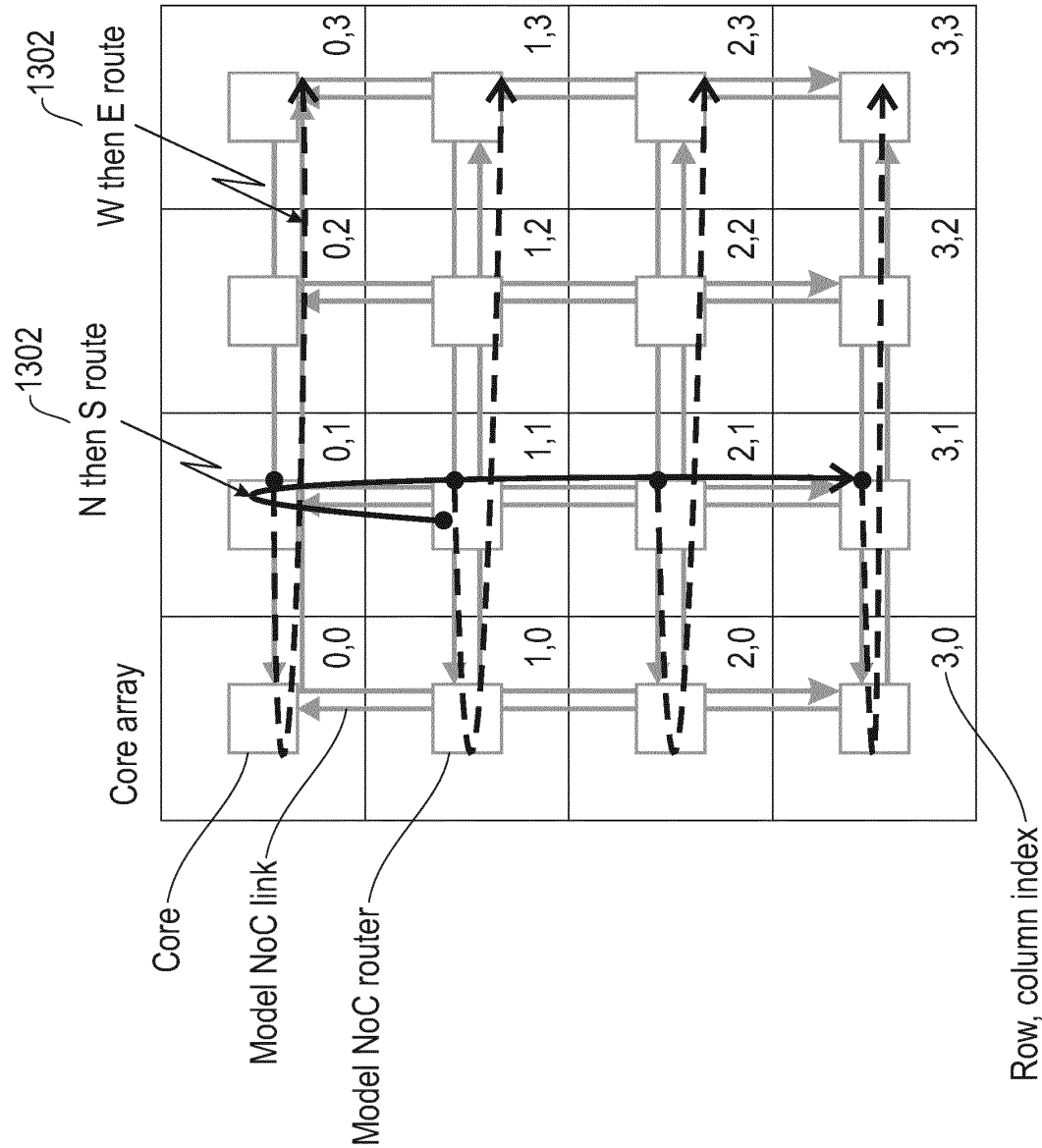


FIG. 13

Signal Name	Width	Definition
addr_dist_mode_Y	1	0 = Y direct address (absolute) 1 = Y distribution flag (multicast) addressing (see Model NoC Addressing slide for usage)
addr_dist_mode_X	1	0 = X direct address (absolute) 1 = X distribution flag (multicast) addressing (see Model NoC Addressing slide for usage)
ext_out_transaction	1	0 = array transaction 1 = external read transaction (data from array to external interface) (see Model NoC External Interface slide for definition/usage)
ext_in_transaction	1	0 = array transaction 1 = external write transaction (data from external interface to array) (see Model NoC External Interface slide for definition/usage)
word_en	4	word enables (for 4X 256b words) (see Unified Memory slides for usage)
addr_valid	1	valid address
addr	10+ 10+ 21	[40:31] = NS address (see Model NoC Addressing slide for definition) [30:21] = EW address (see Model NoC Addressing slide for definition) [20:0] = local core address
data_valid	1	valid data
data	1024	data

FIG. 14

See: CORE_MNOC_CONFIG_REG

1501

Field:	Reserved	Distr Row ID
Width:	6	4
Bits:	9:4	3:0

1502

Field:	Reserved	Distr Col ID
Width:	6	4
Bits:	9:4	3:0

1503

Field:	Boolean Neg	Any All Select	Distr Flags
Width:	1	1	8
Bits:	9	8	7:0

Boolean Neg	
0	Direct Boolean match expression (no negation)
1	Invert (negate) Boolean match expression

Any All SEL	
0	Any match expression
1	All match expression

FIG. 15

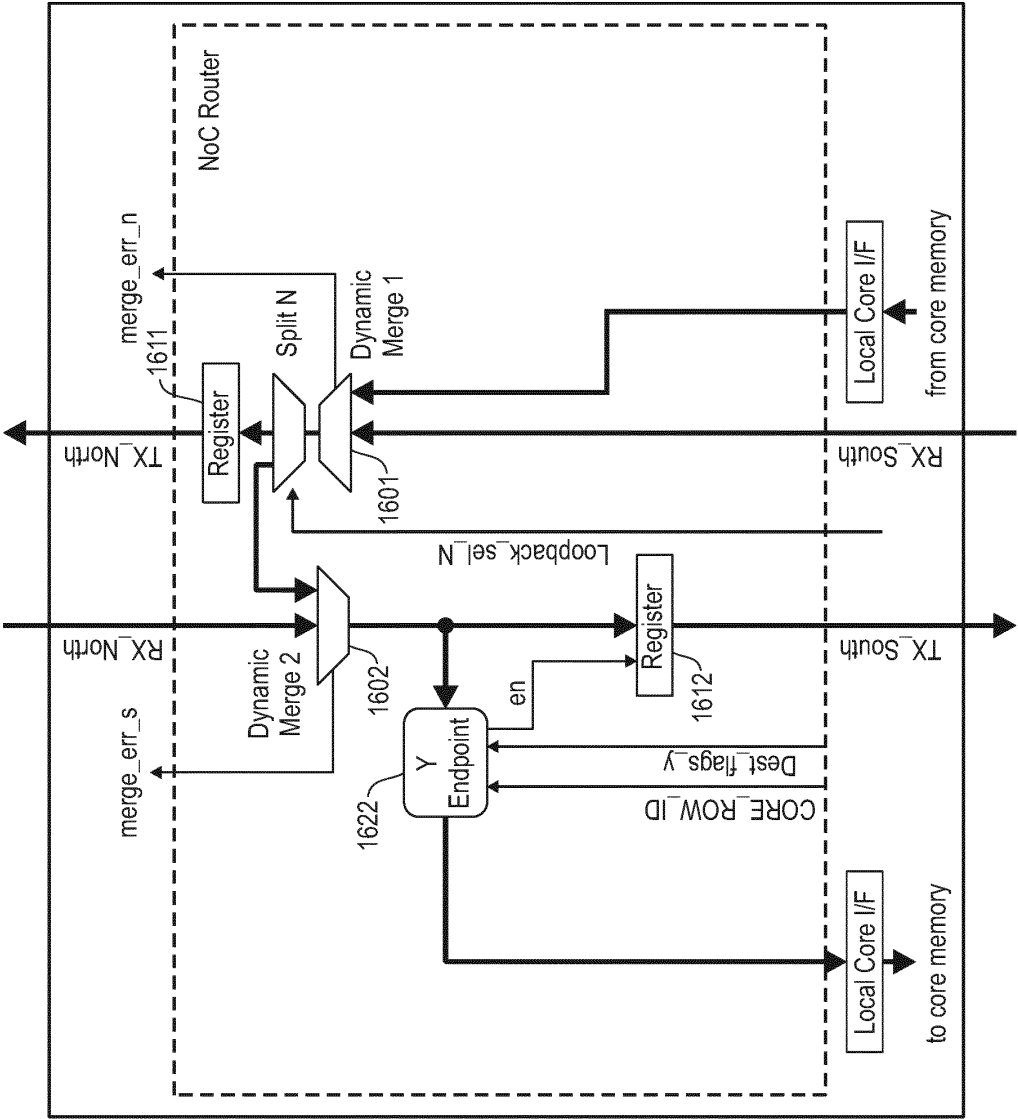


FIG. 16

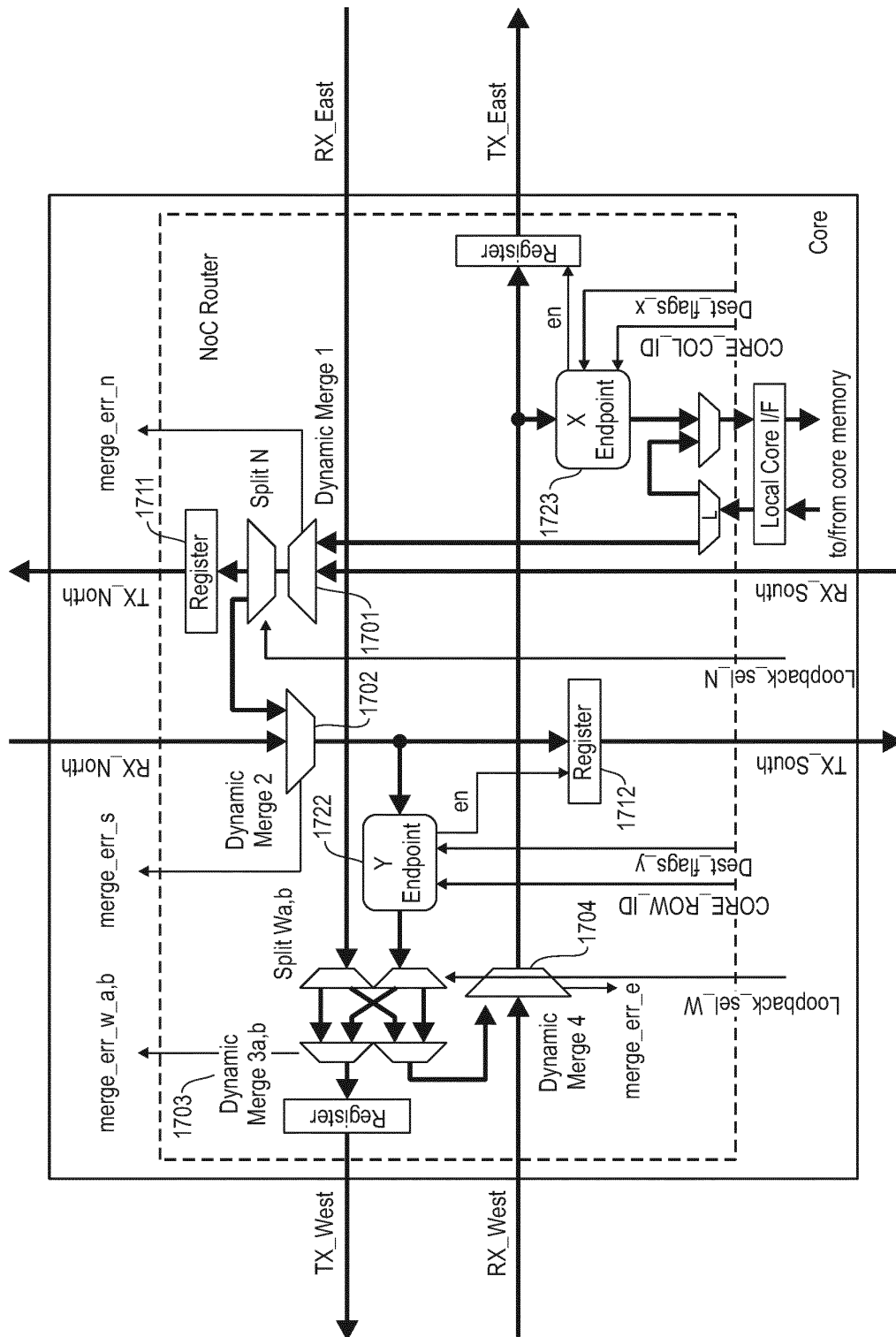


FIG. 17

Entry	Exit	Path	Cycles
RX_West	TX_East	(Strait-through)	1
RX_West	Local Core I/F	X Addr match	1
RX_East	TX_West	(Strait-through)	1
RX_East	TX_East	West Loopback	1
RX_East	Local Core I/F	West Loopback → X Addr match	1
RX_North	TX_South	(Strait-through)	1
RX_North	TX_West	Y Addr match	2
RX_North	TX_East	Y Addr match → West Loopback	2
RX_North	Local Core I/F	Y Addr match → West Loopback → X Addr match	2

FIG. 18A

Entry	Exit	Path	Cycles
RX_South	TX_North	(Strait-through)	1
RX_South	TX_South	North Loopback	1
RX_South	TX_West	North Loopback → Y Addr match	2
RX_South	TX_East	North Loopback → Y Addr match → West Loopback	2
RX_South	Local Core I/F	North Loopback → Y Addr match → West Loopback → X Addr match	2
Local Core I/F	TX_North	(Strait-through)	1
Local Core I/F	TX_South	North Loopback	1
Local Core I/F	TX_West	North Loopback → Y Addr match	2
Local Core I/F	TX_East	North Loopback → Y Addr match → West Loopback	2
Local Core I/F (multicast)	Local Core I/F	North Loopback → Y Addr match → West Loopback → X Addr match	2
Local Core I/F (direct)	Local Core I/F	Local Core I/F (does not enter MNoC Router)	--

FIG. 18B

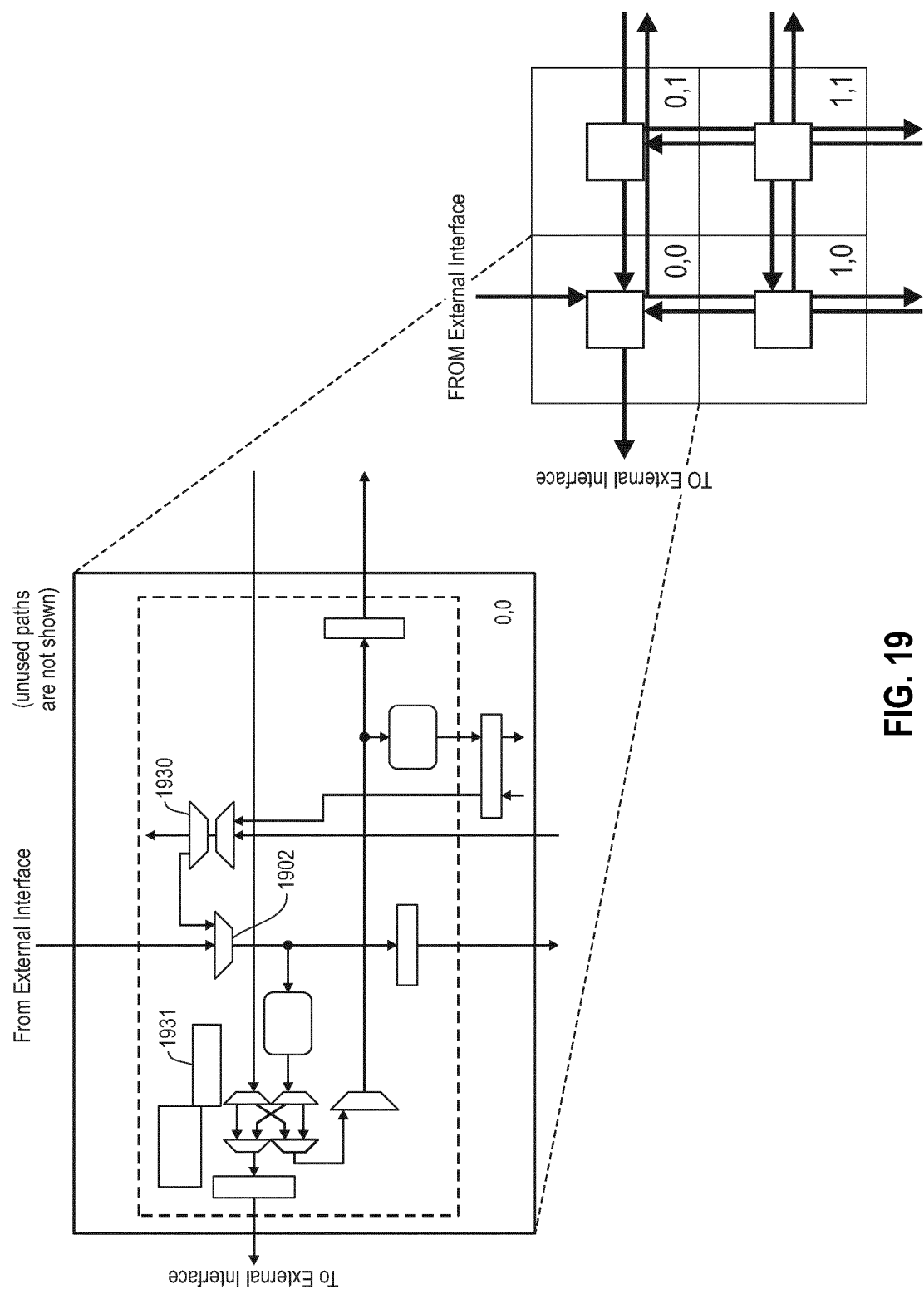


FIG. 19

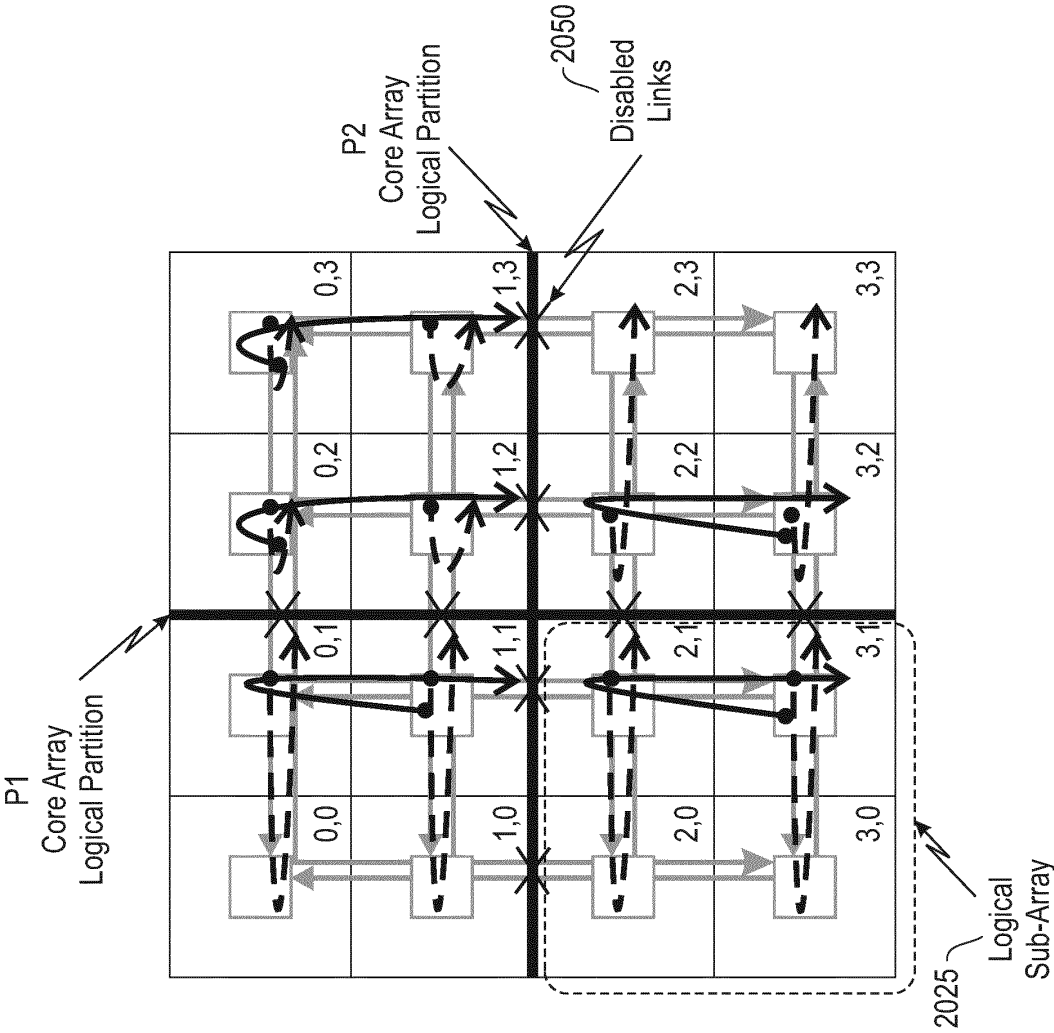


FIG. 20

Mode	Interface	Link Disable	Loopback	Data Transactions	External Transactions
Normal, Interior	{N,S,E,W} TX, RX	0	0	pass	pass
Normal, top edge (row 0)	N TX	0	1	loopback	loopback
Normal, top edge	N RX	0	1	zero	pass
Normal, left edge (col 0)	W TX	0	1	loopback	ext_out: pass ext_in: loopback
Normal, left edge	W RX	0	1	zero	zero
Normal, bottom edge (row N-1)	S TX	0	--	drop	drop
Normal, bottom edge	S RX	0	--	zero	zero
Normal, right edge (col N-1)	E TX	0	--	drop	drop
Normal, right edge	E RX	0	--	zero	zero
Partition, Interior	{N,S,E,W} TX, RX	0	0	pass	pass
Partition, top edge	N TX	1	1	loopback	pass
Partition, top edge	N RX	1	1	zero (drop)	pass
Partition, left edge	W TX	1	1	loopback	pass
Partition, left edge	W RX	1	1	zero (drop)	pass
Partition, bottom edge	S TX	1	--	drop	pass
Partition, bottom edge	S RX	1	--	zero (drop)	pass
Partition, right edge	E TX	1	--	drop	pass
Partition, right edge	E RX	1	--	zero (drop)	pass

FIG. 21A

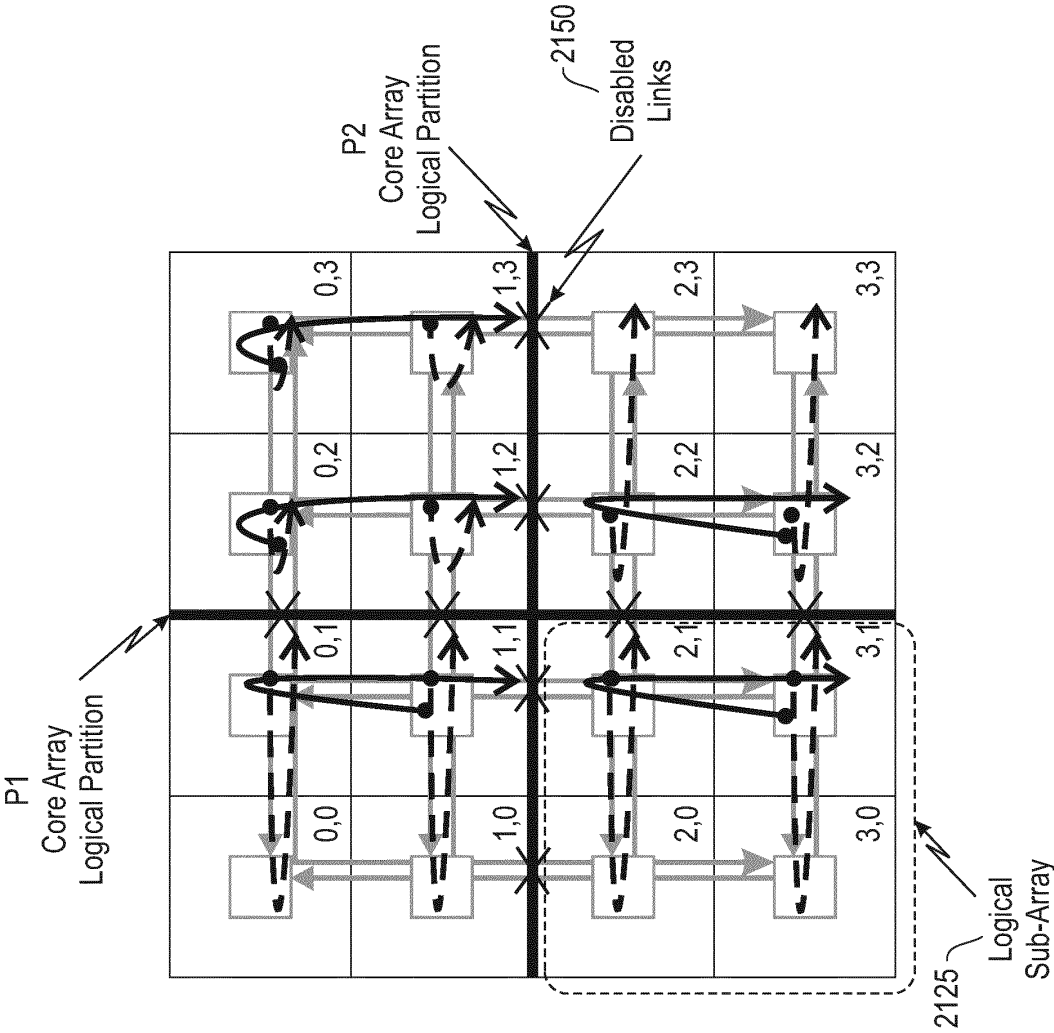


FIG. 21B

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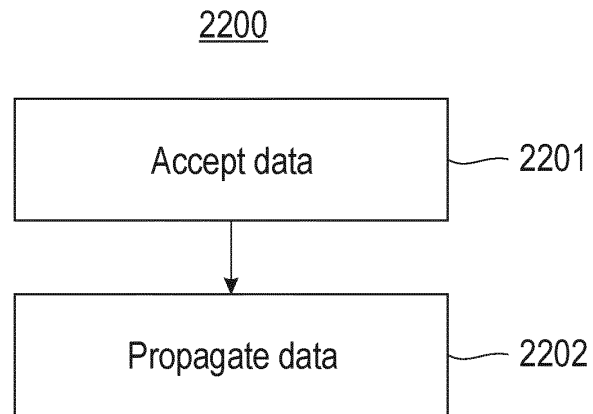


FIG. 22

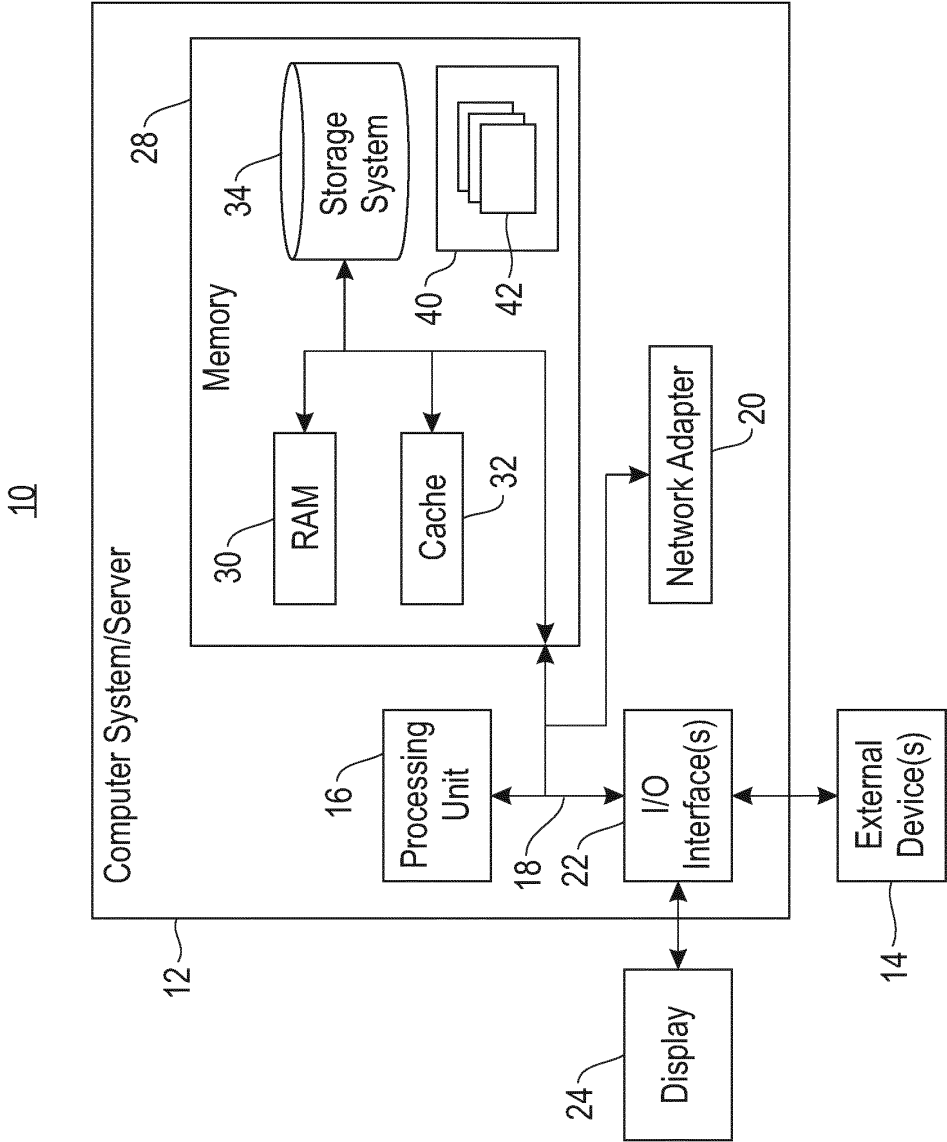


FIG. 23