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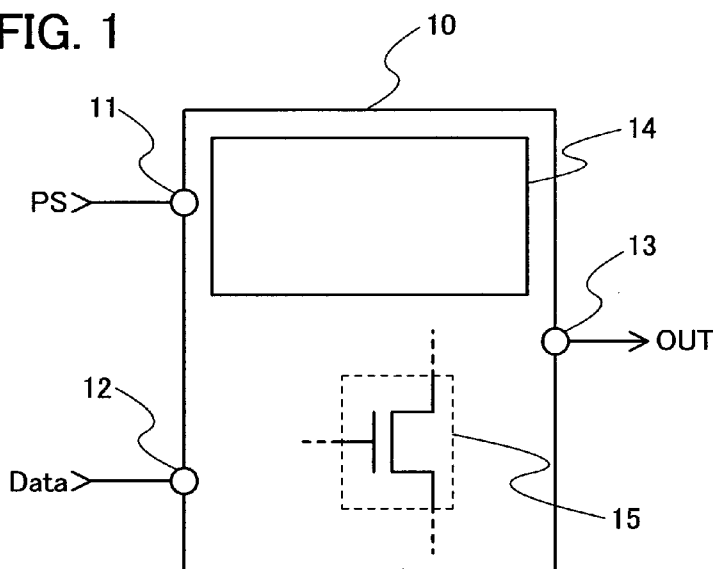
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(54) Title: LOGIC CIRCUIT AND SEMICONDUCTOR DEVICE

FIG. 1



(57) Abstract: In a logic circuit where clock gating is performed, the standby power is reduced or malfunction is suppressed. The logic circuit includes a transistor which is in an off state where a potential difference exists between a source terminal and a drain terminal over a period during which a clock signal is not supplied. A channel formation region of the transistor is formed using an oxide semiconductor in which the hydrogen concentration is reduced. Specifically, the hydrogen concentration of the oxide semiconductor is 5×10^{19} (atoms/cm³) or lower. Thus, leakage current of the transistor can be reduced. As a result, in the logic circuit, reduction in standby power and suppression of malfunction can be achieved.