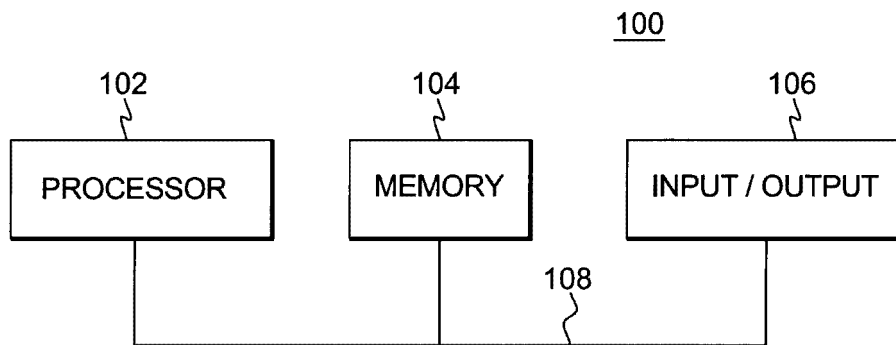
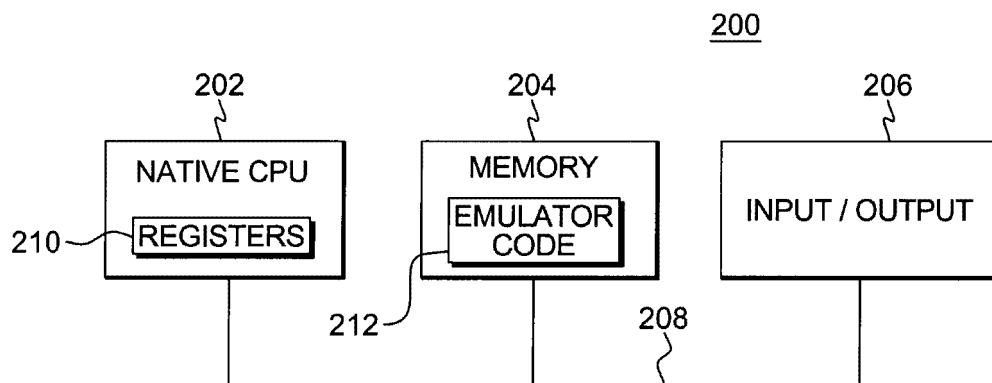
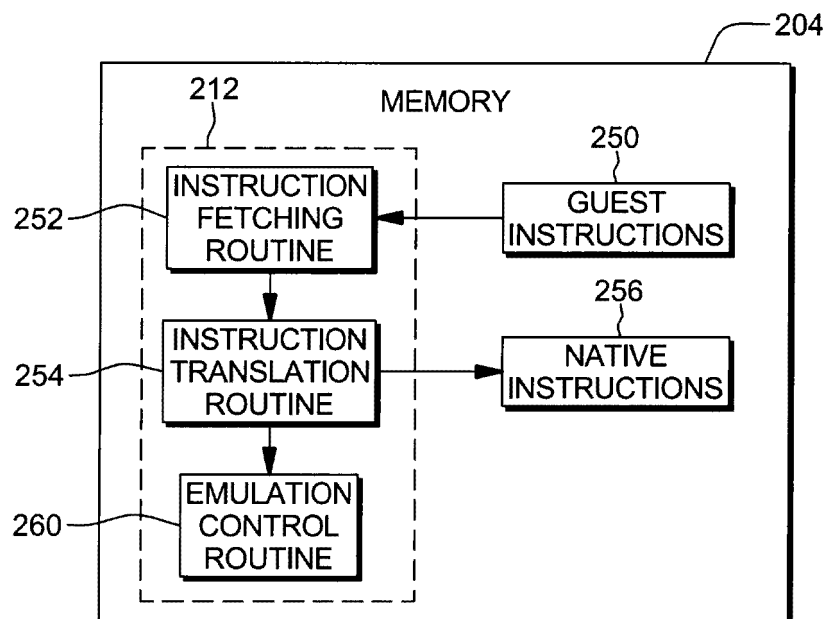




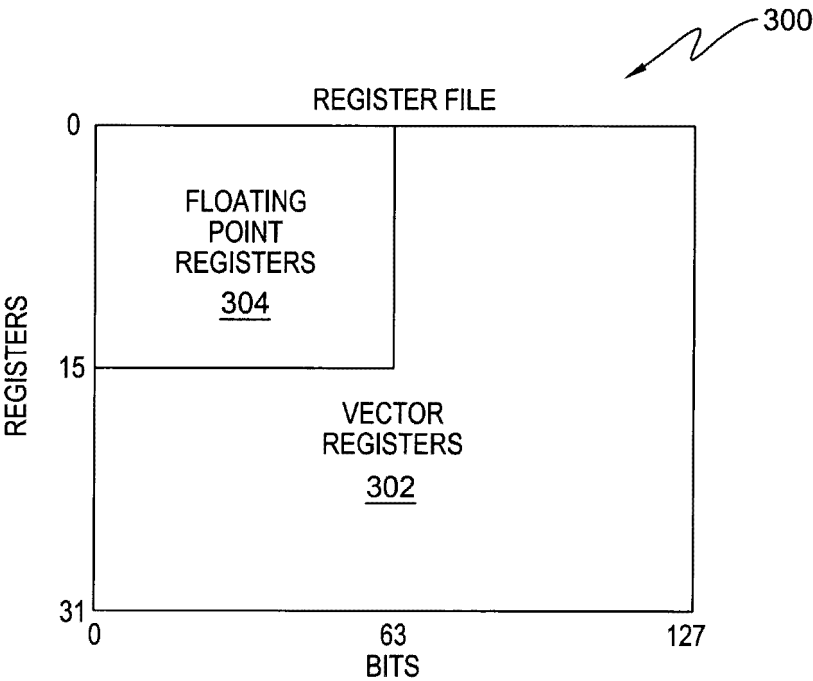


FIG. 3

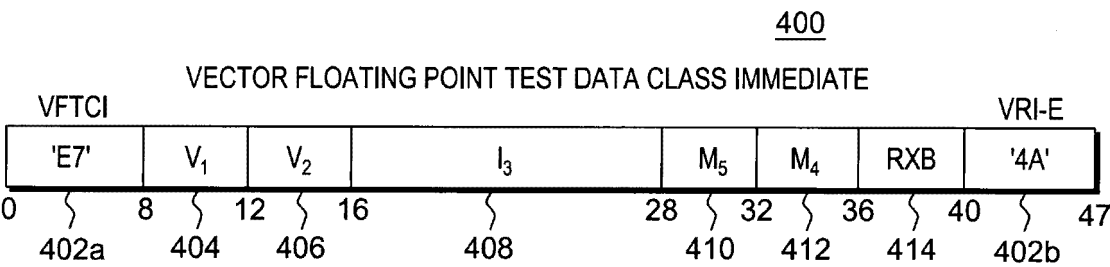


FIG. 4A

BFP ELEMENT CLASS	BIT USED WHEN SIGN IS	
	+	-
ZERO	0	1
NORMAL NUMBER	2	3
SUBNORMAL NUMBER	4	5
INFINITY	6	7
QUIET NAN	8	9
SIGNALING NAN	10	11

FIG. 4B

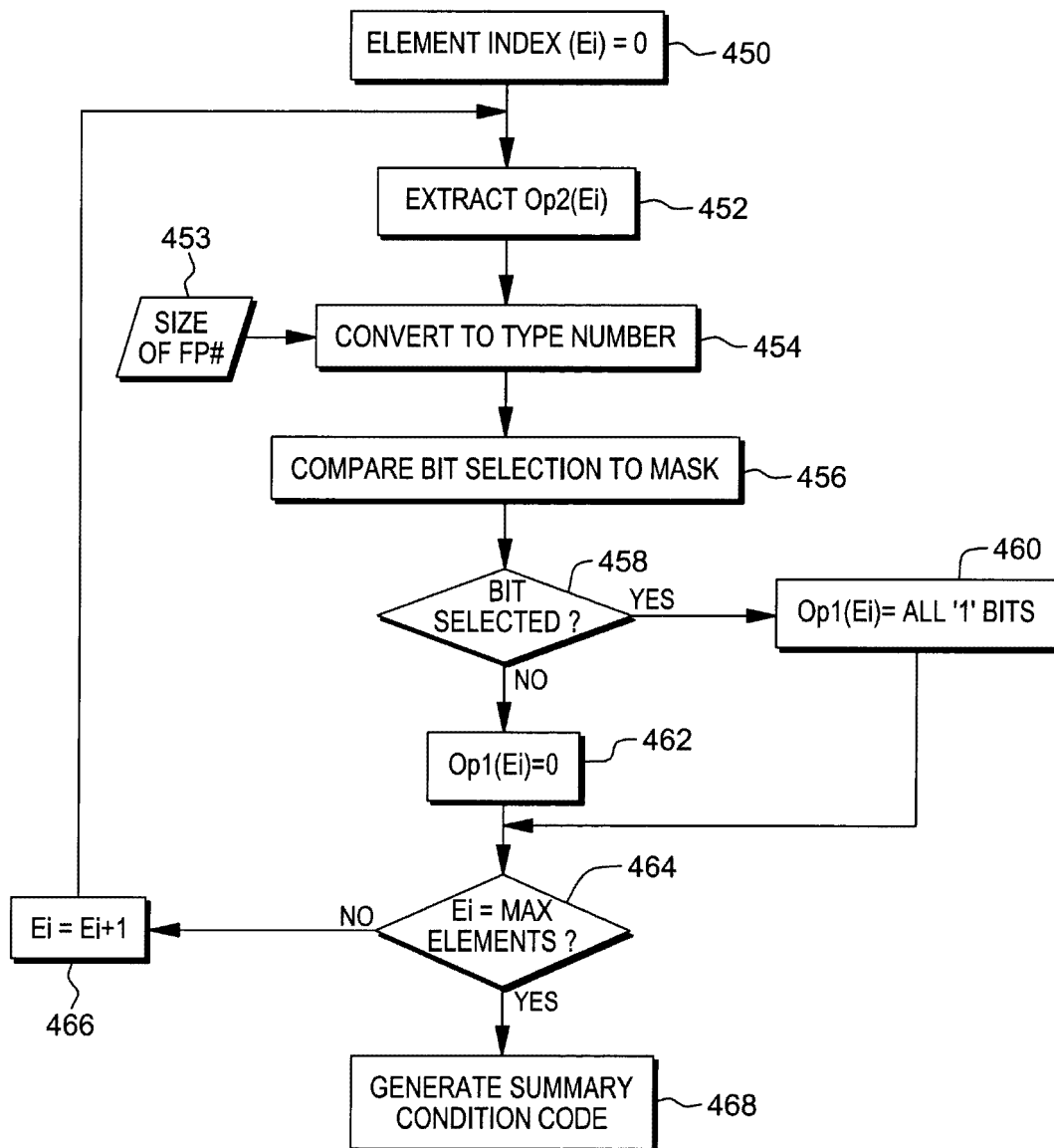


FIG. 4C

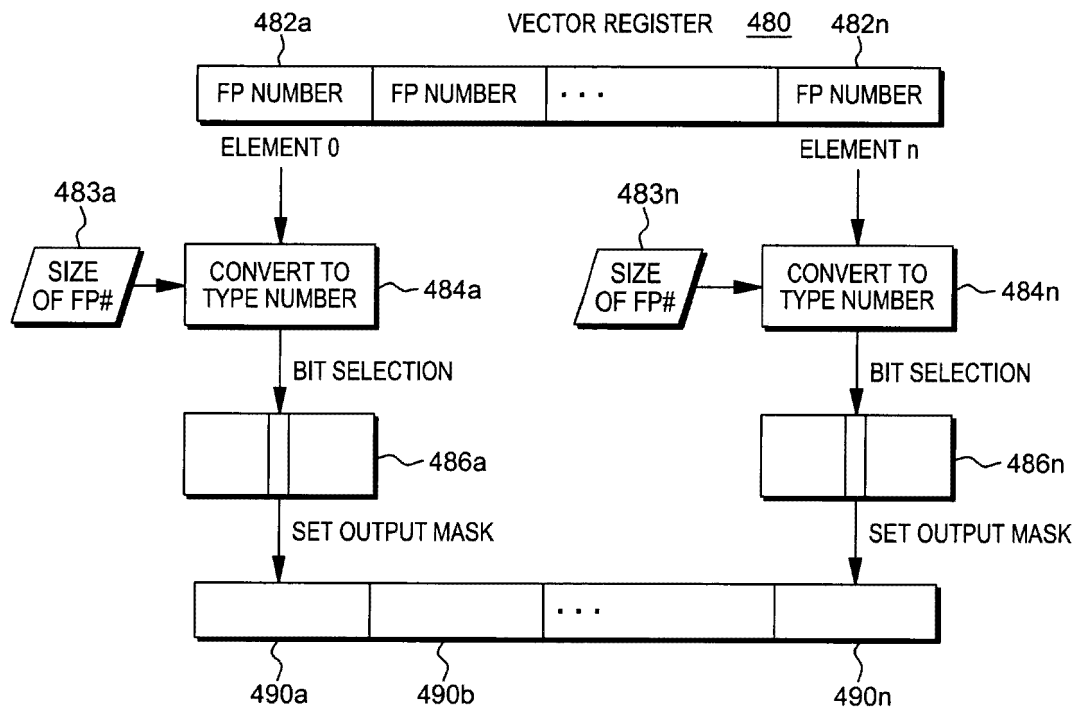


FIG. 4D

ENTITY	SIGN	BIASED EXONENT	UNIT BIT *	FRACTION
TRUE ZERO	$\pm$	0	0	0
DENORMALIZED NUMBERS	$\pm$	0**	0	NOT 0
NORMALIZED NUMBERS	$\pm$	NOT 0, NOT ALL ONES	1	ANY
INFINITY	$\pm$	ALL ONES	-	0
QUIET NAN	$\pm$	ALL ONES	-	FO=1, Fr=ANY
SIGNALING NAN	$\pm$	ALL ONES	-	FO=0, Fr $\neq$ 0
EXPLANATION:				
* THE UNIT BIT IS IMPLIED				
** THE BIASED EXONENT IS TREATED ARITHMETICALLY AS IF IT HAD THE VALUE ONE				
NAN NOT A NUMBER				
FO LEFTMOST BIT OF FRACTION				
Fr REMAINING BITS OF FRACTION				

FIG. 4E

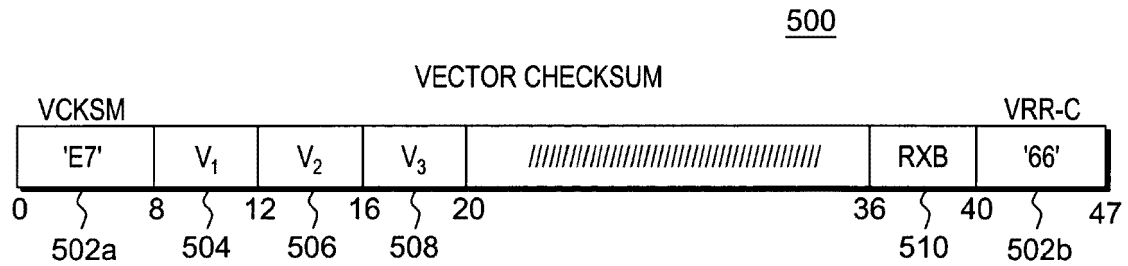


FIG. 5A

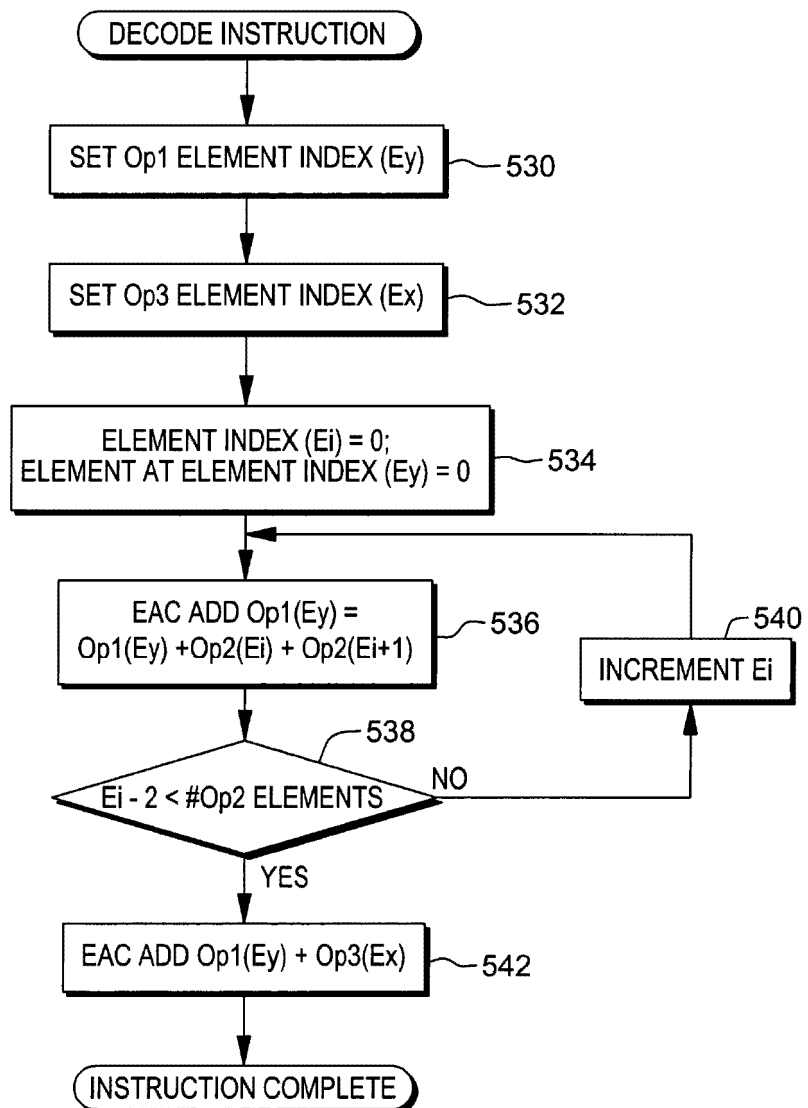


FIG. 5B

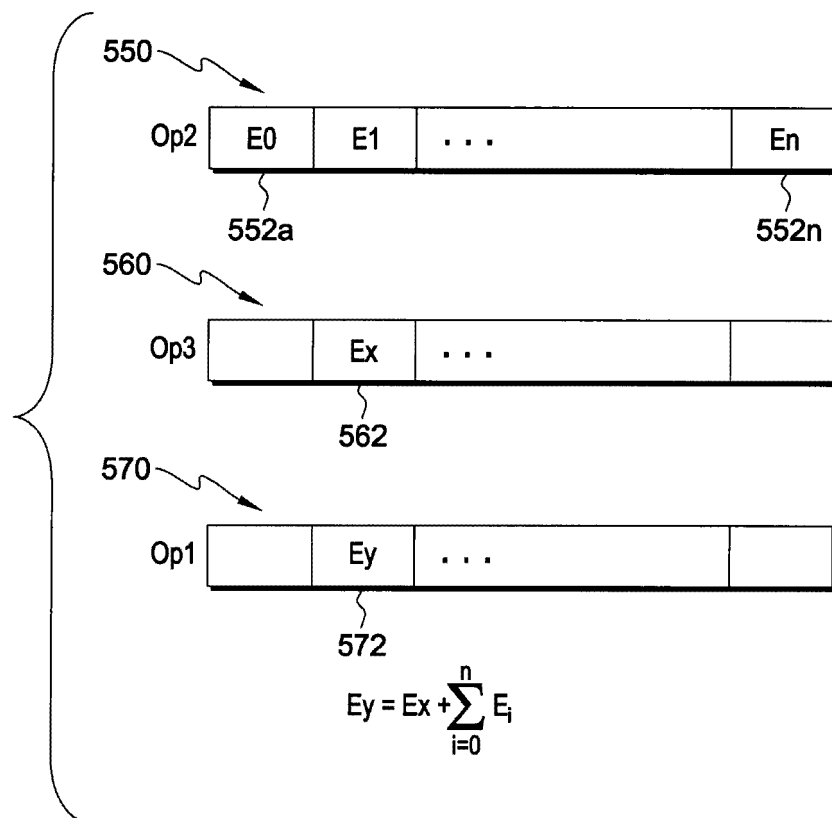


FIG. 5C

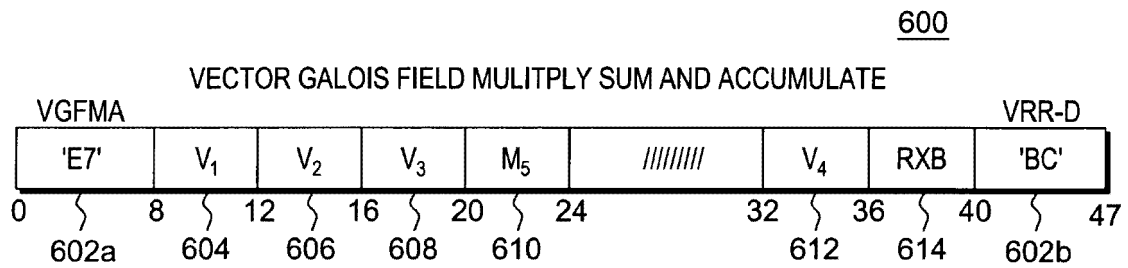


FIG. 6A

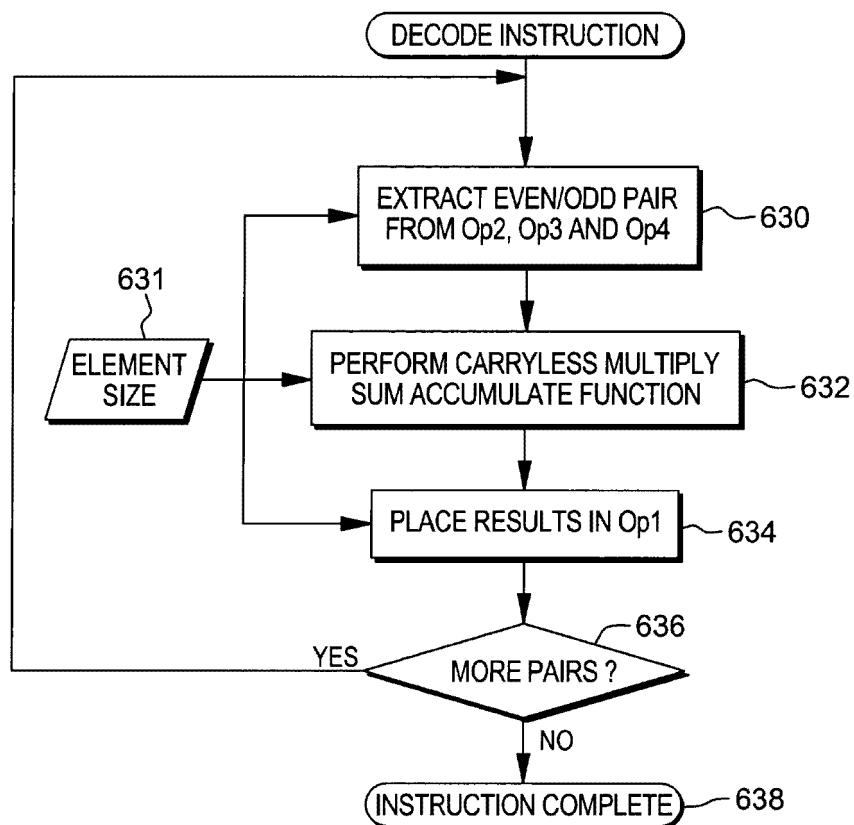


FIG. 6B

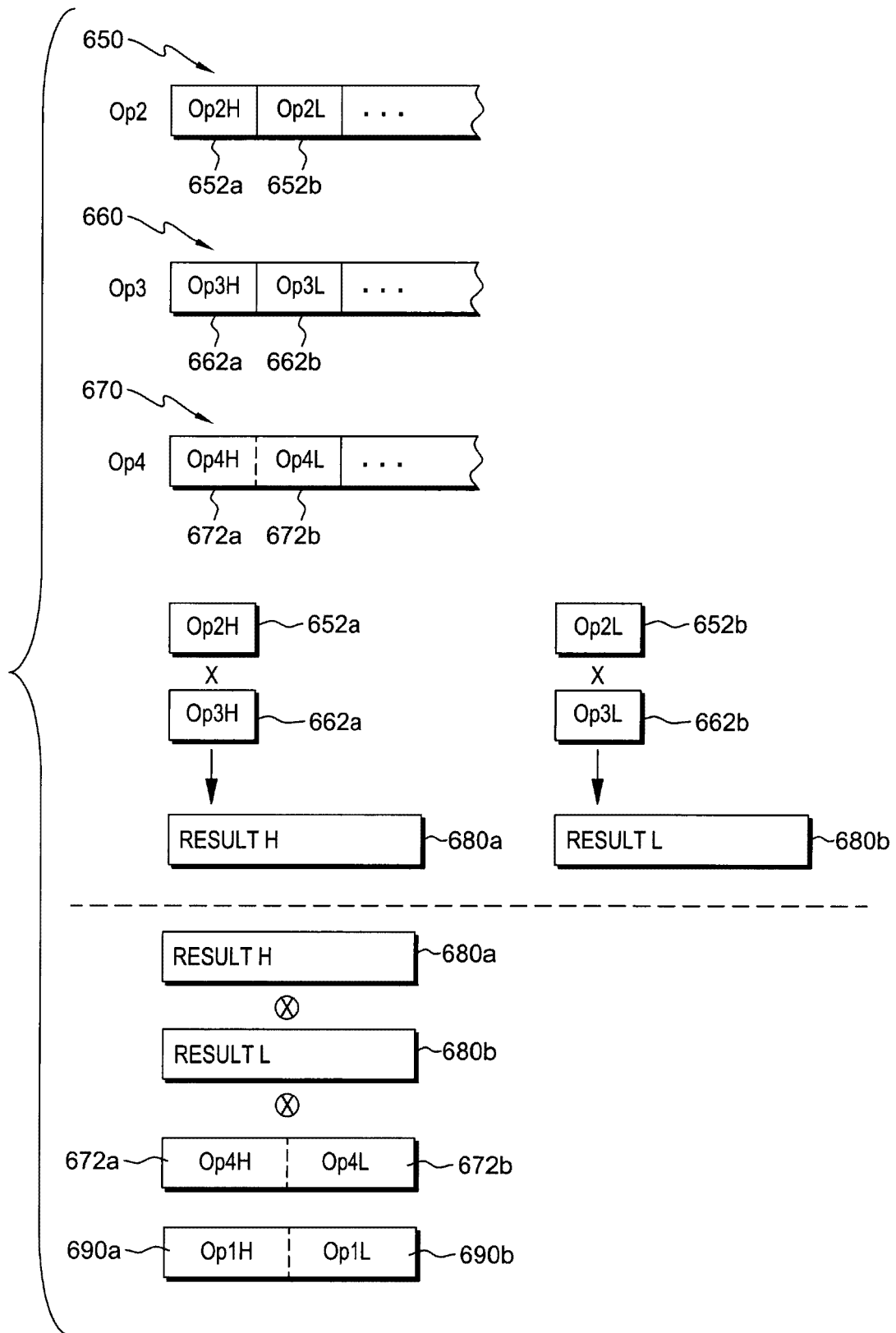


FIG. 6C

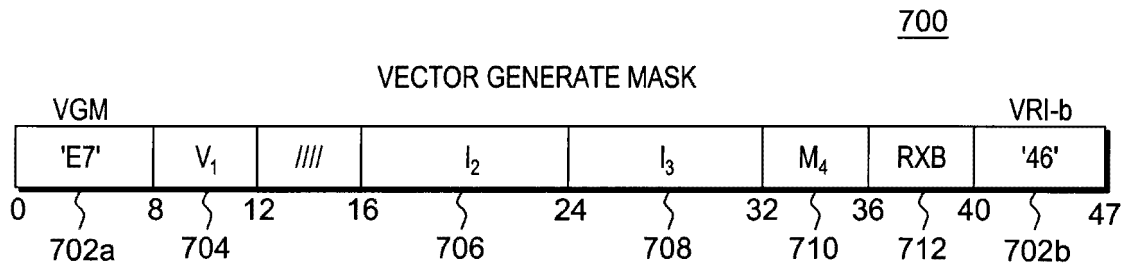


FIG. 7A

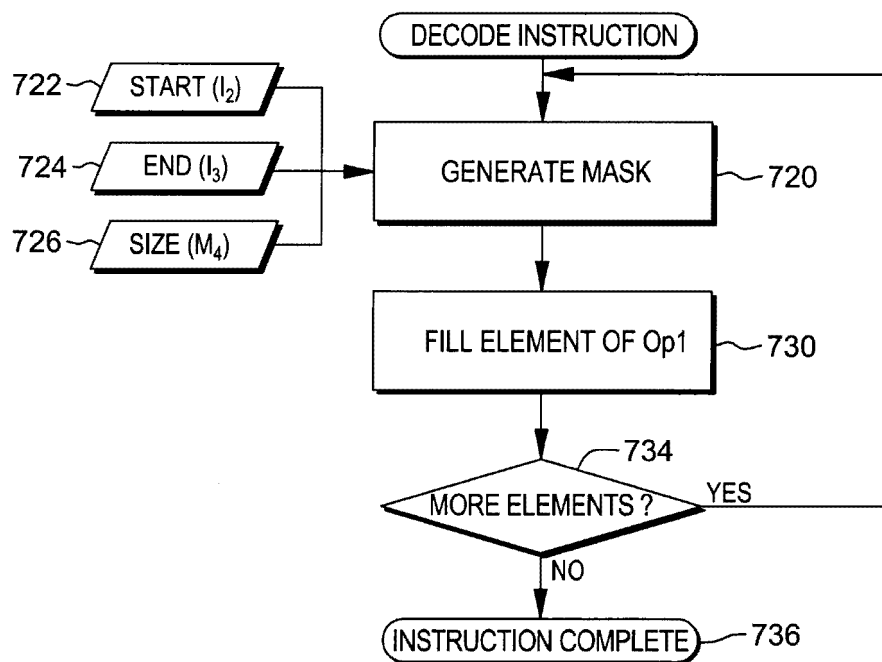


FIG. 7B

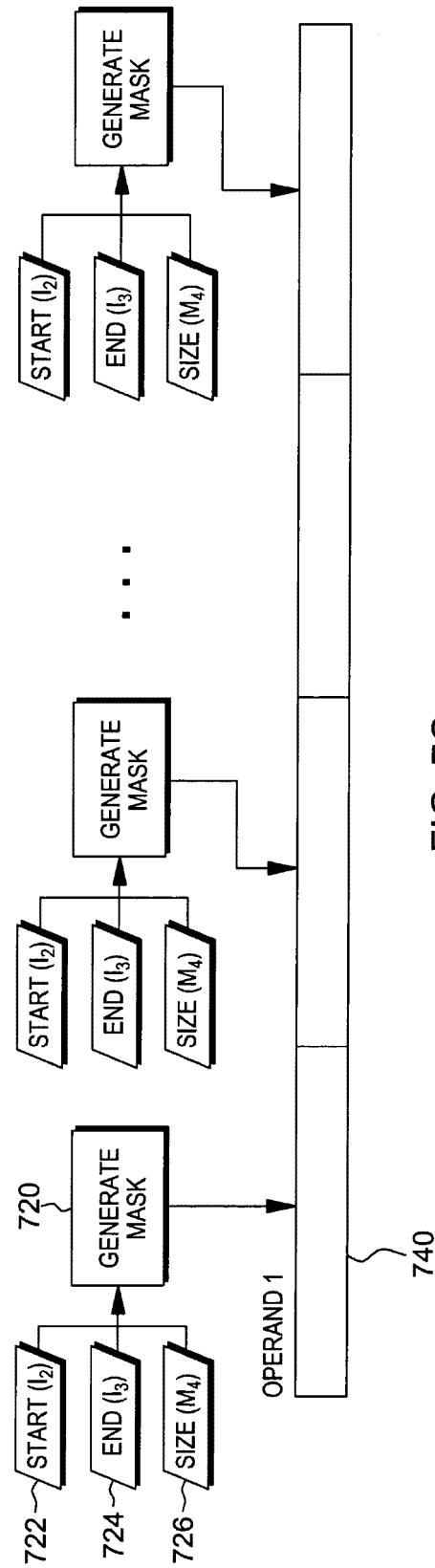


FIG. 7C

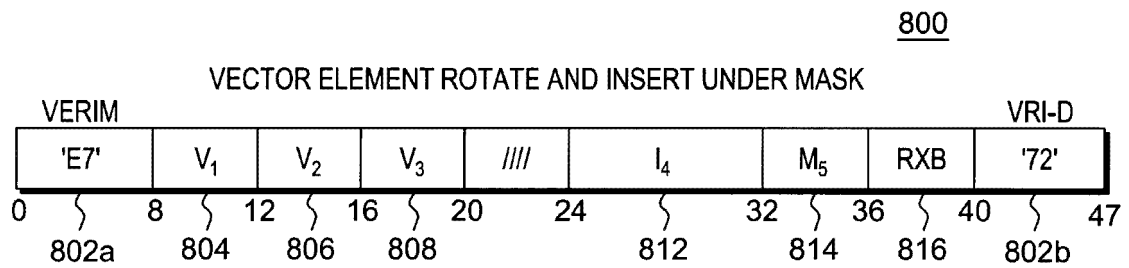


FIG. 8A

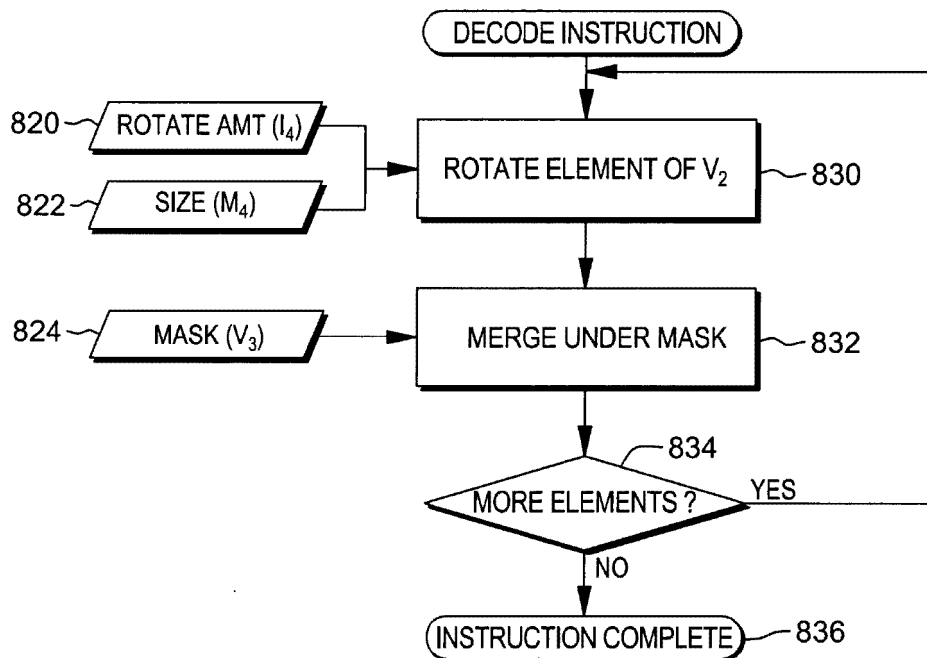


FIG. 8B

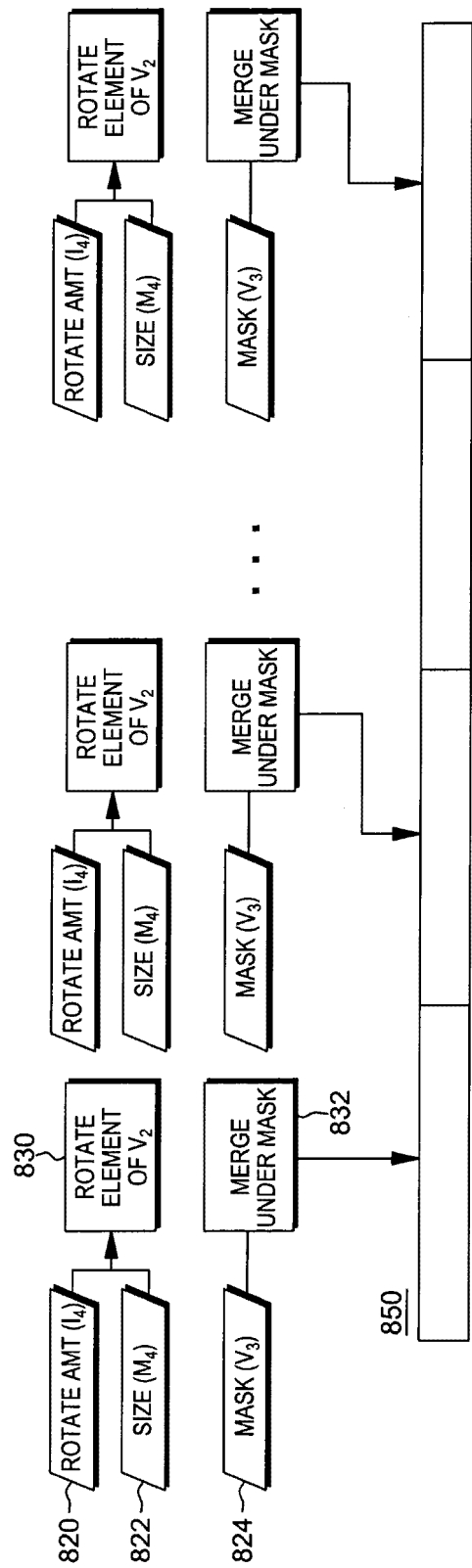


FIG. 8C

900

VECTOR EXCEPTION CODE

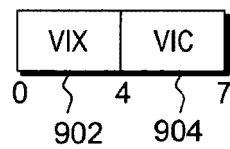


FIG. 9A

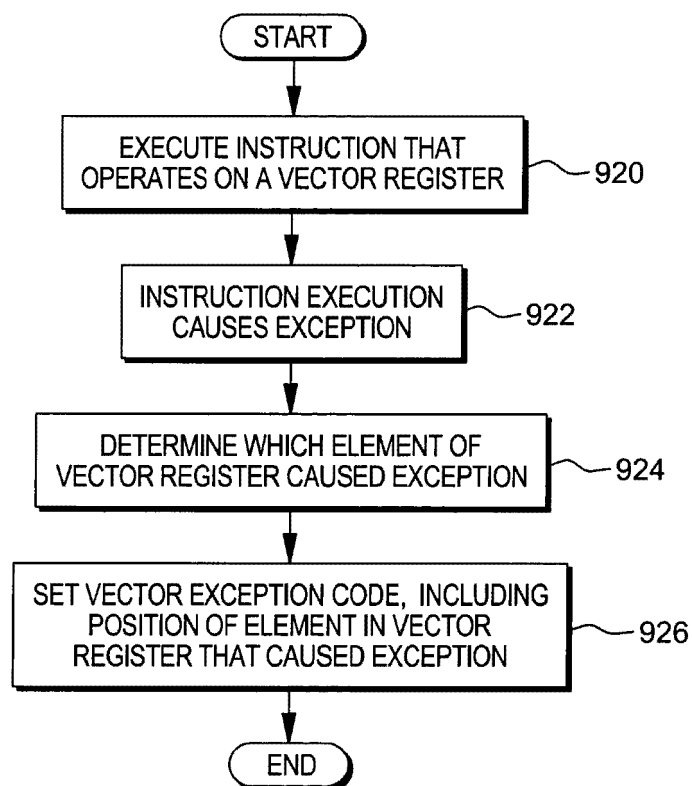


FIG. 9B

COMPUTER
PROGRAM
PRODUCT
1000

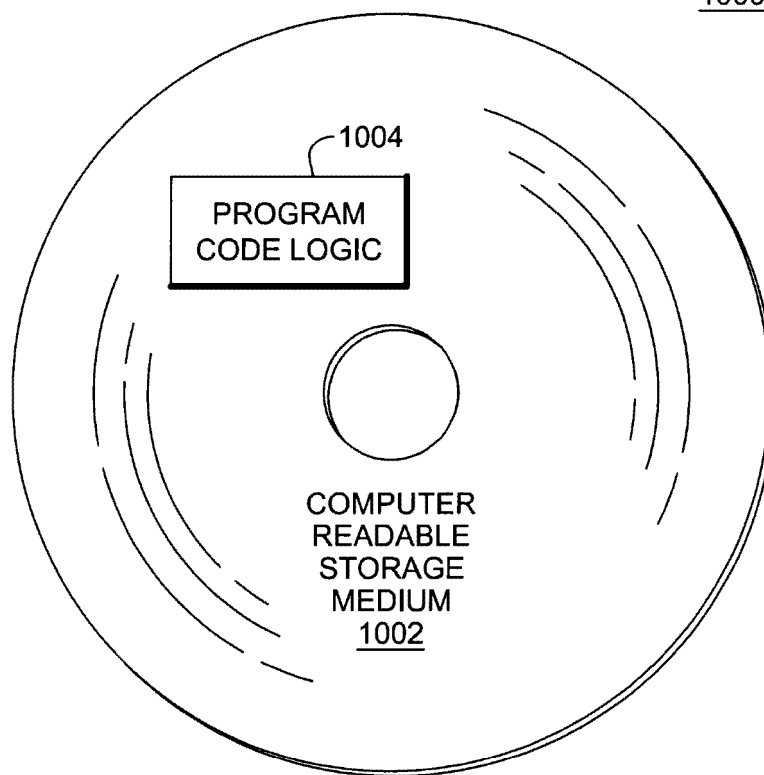


FIG. 10

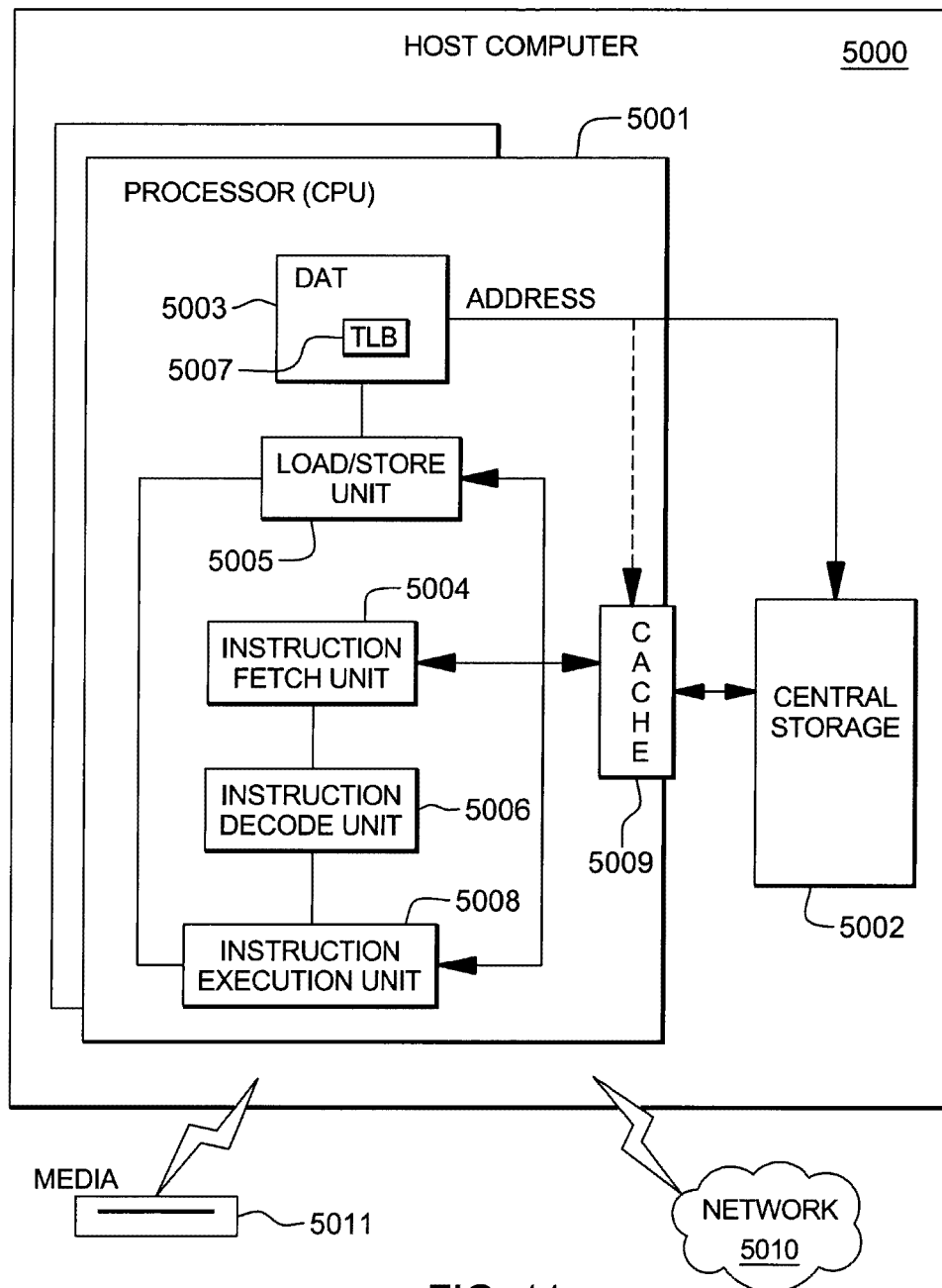


FIG. 11

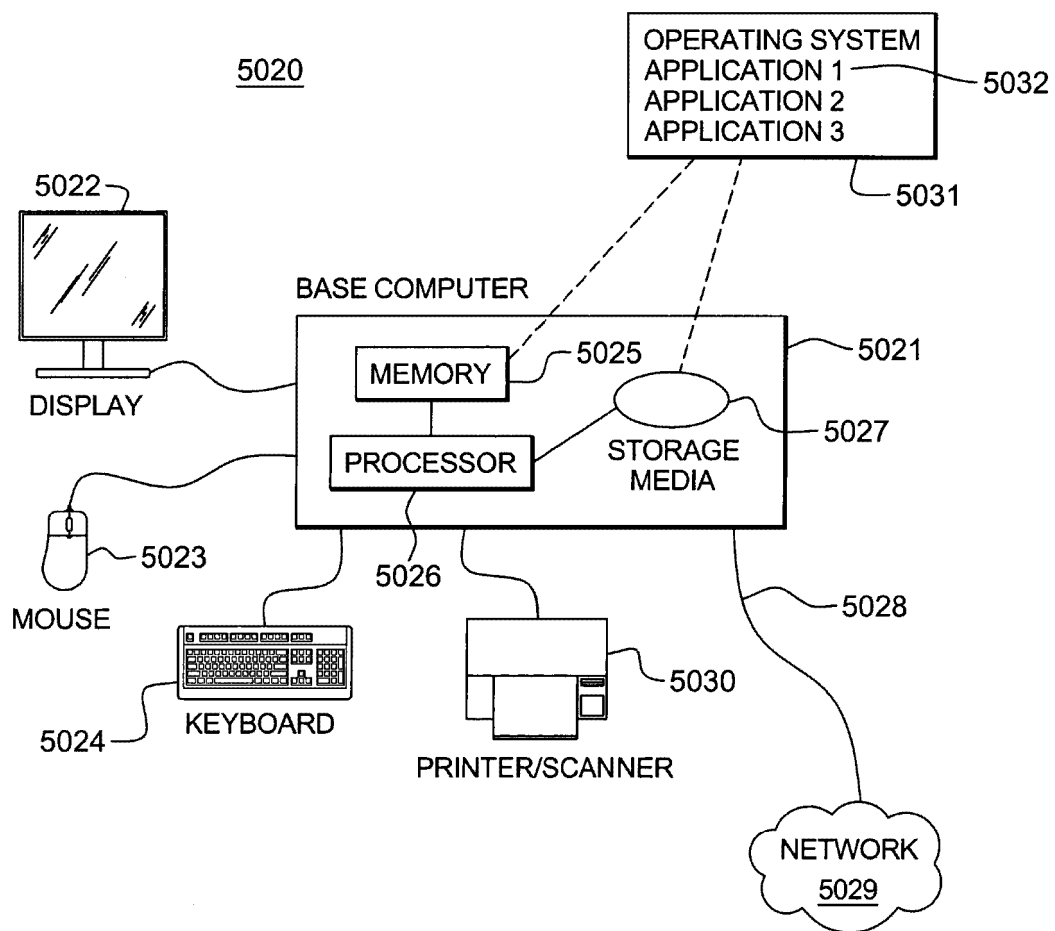


FIG. 12

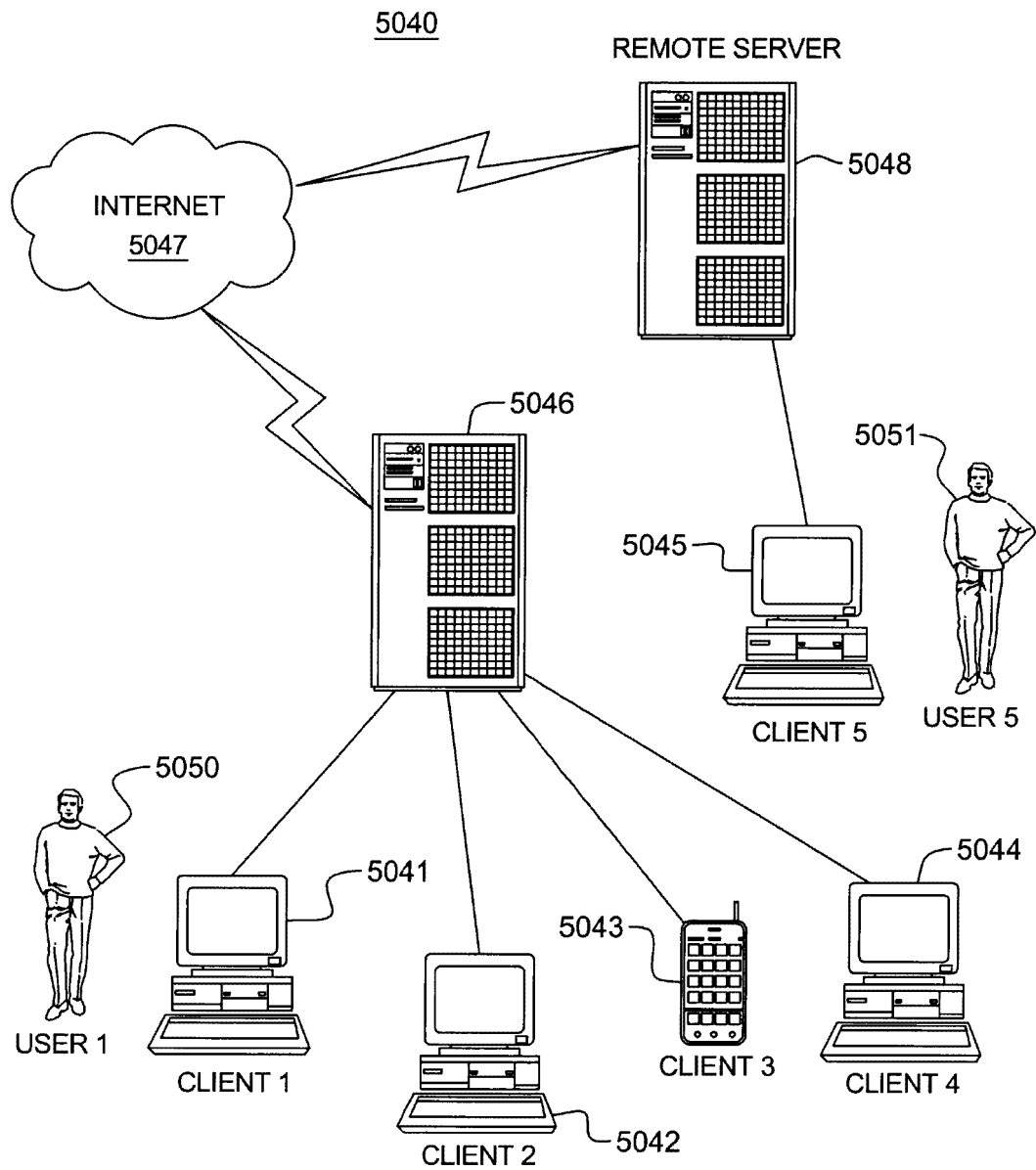


FIG. 13

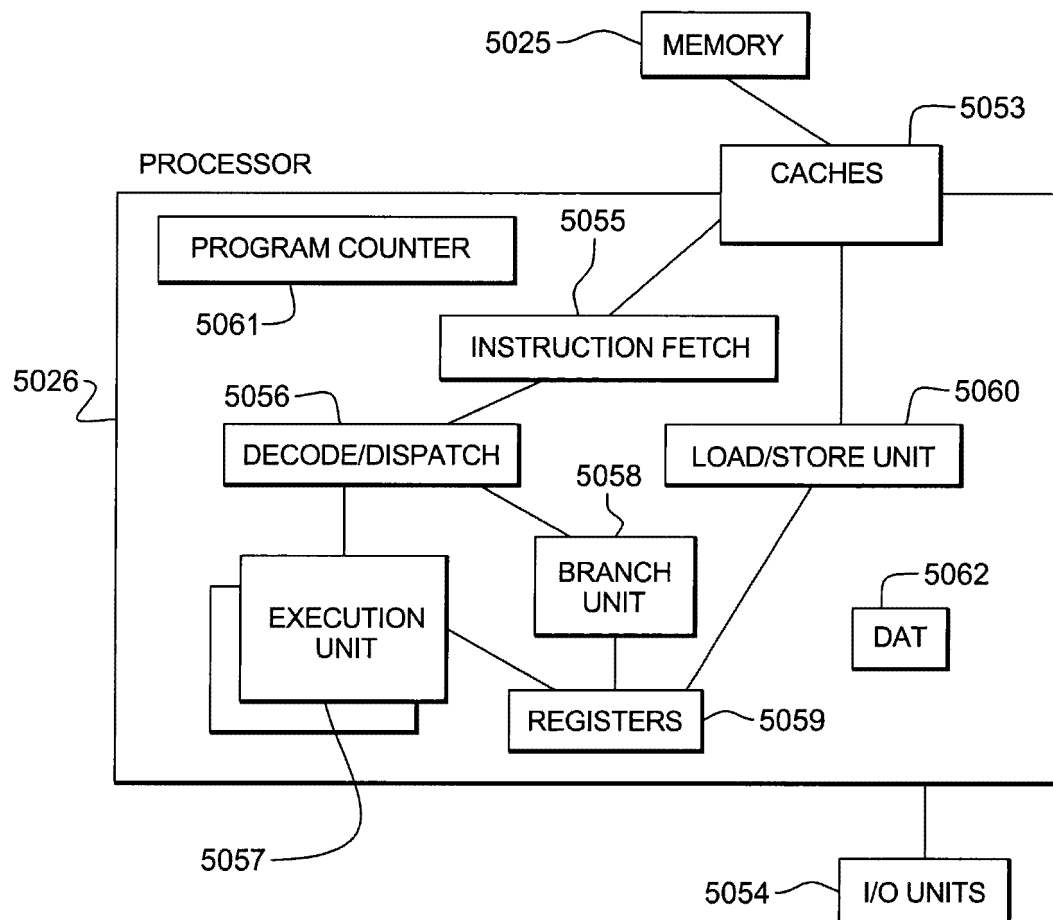


FIG. 14

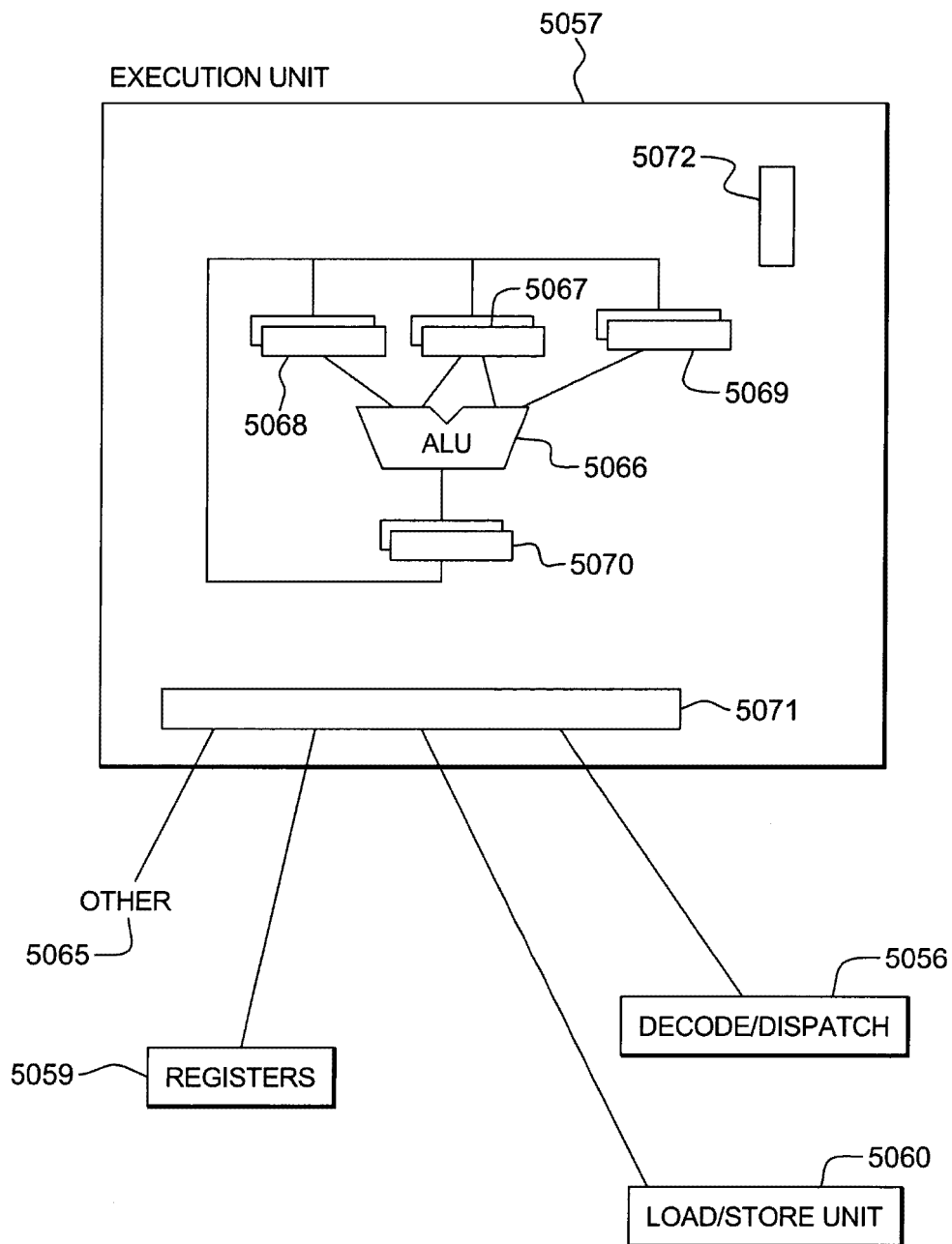


FIG. 15A

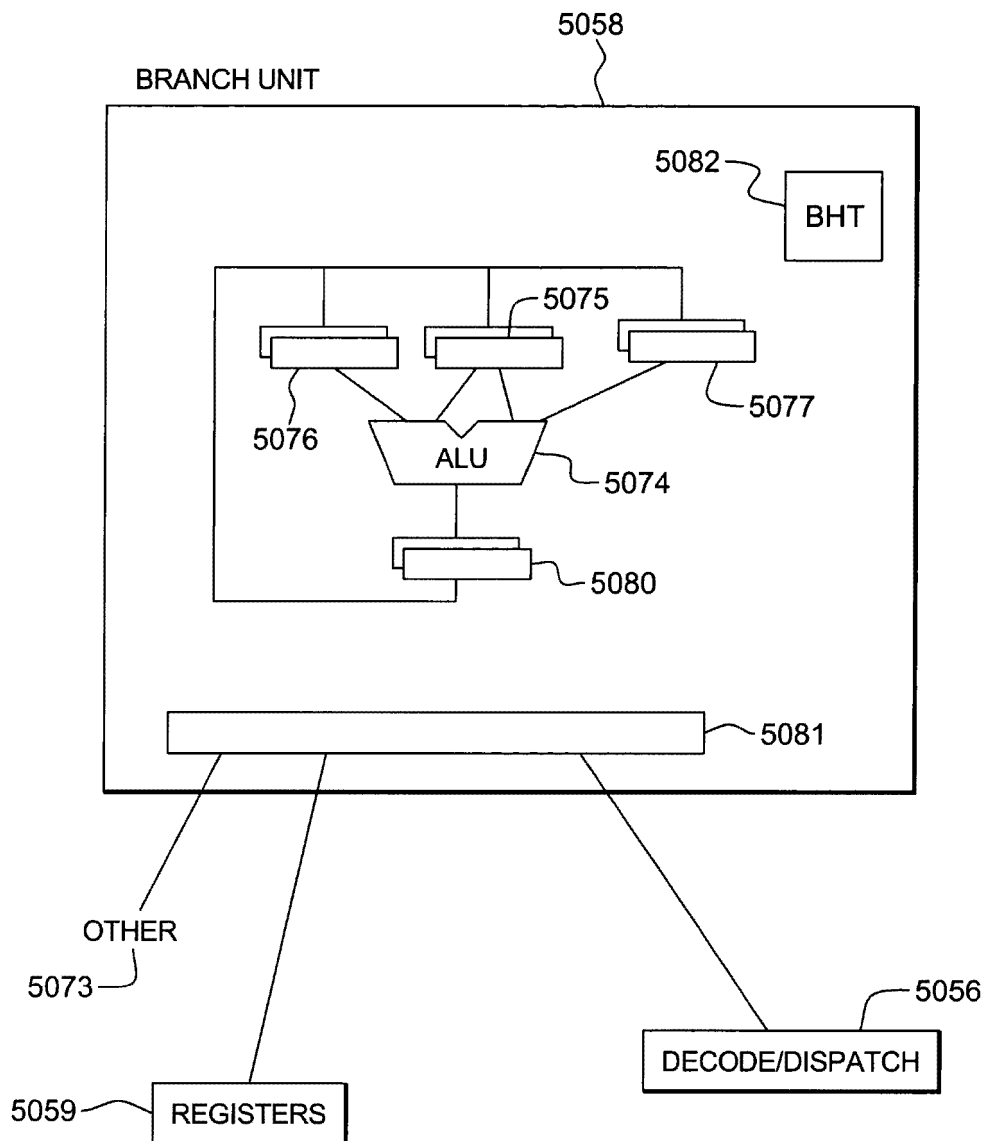


FIG. 15B

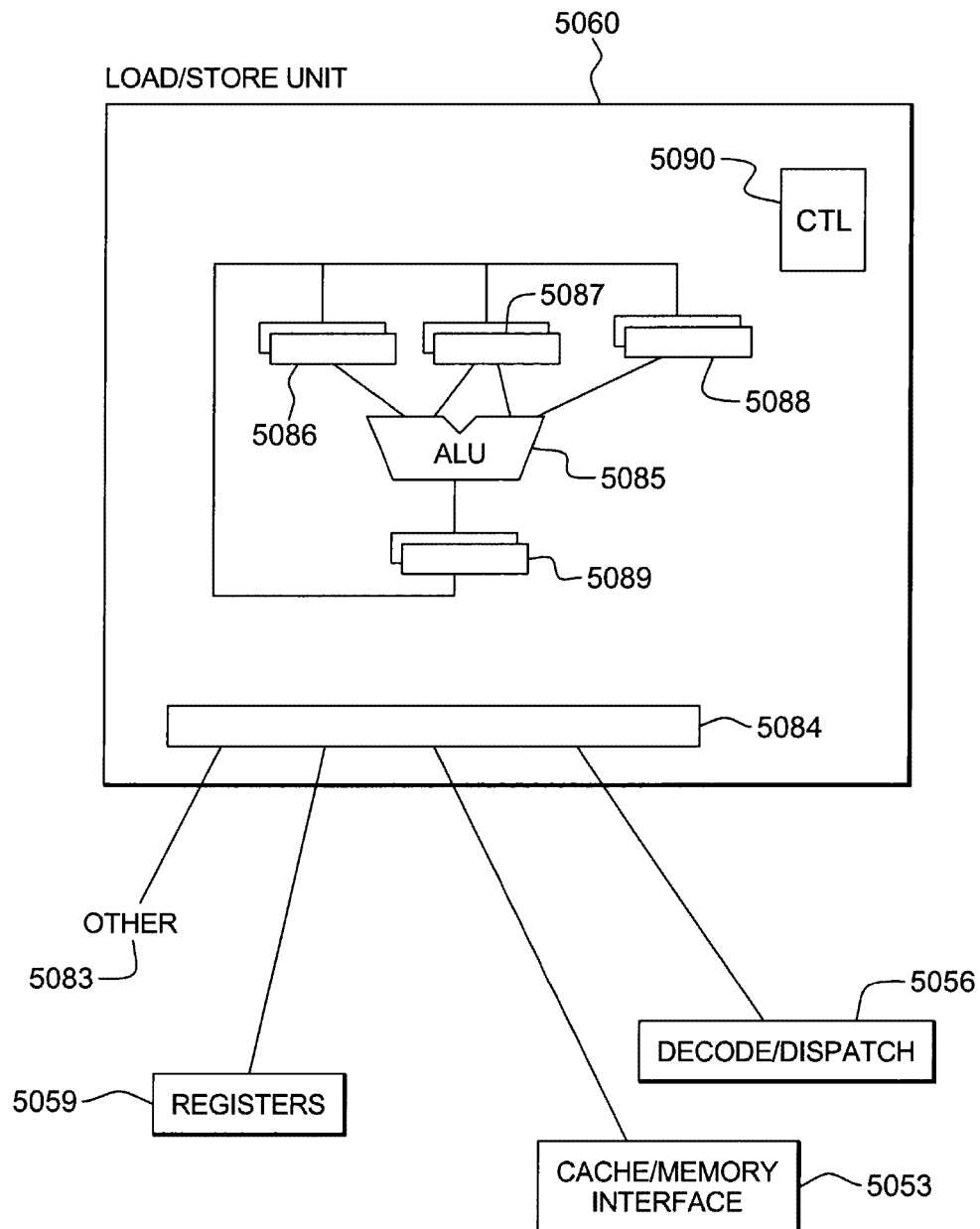


FIG. 15C

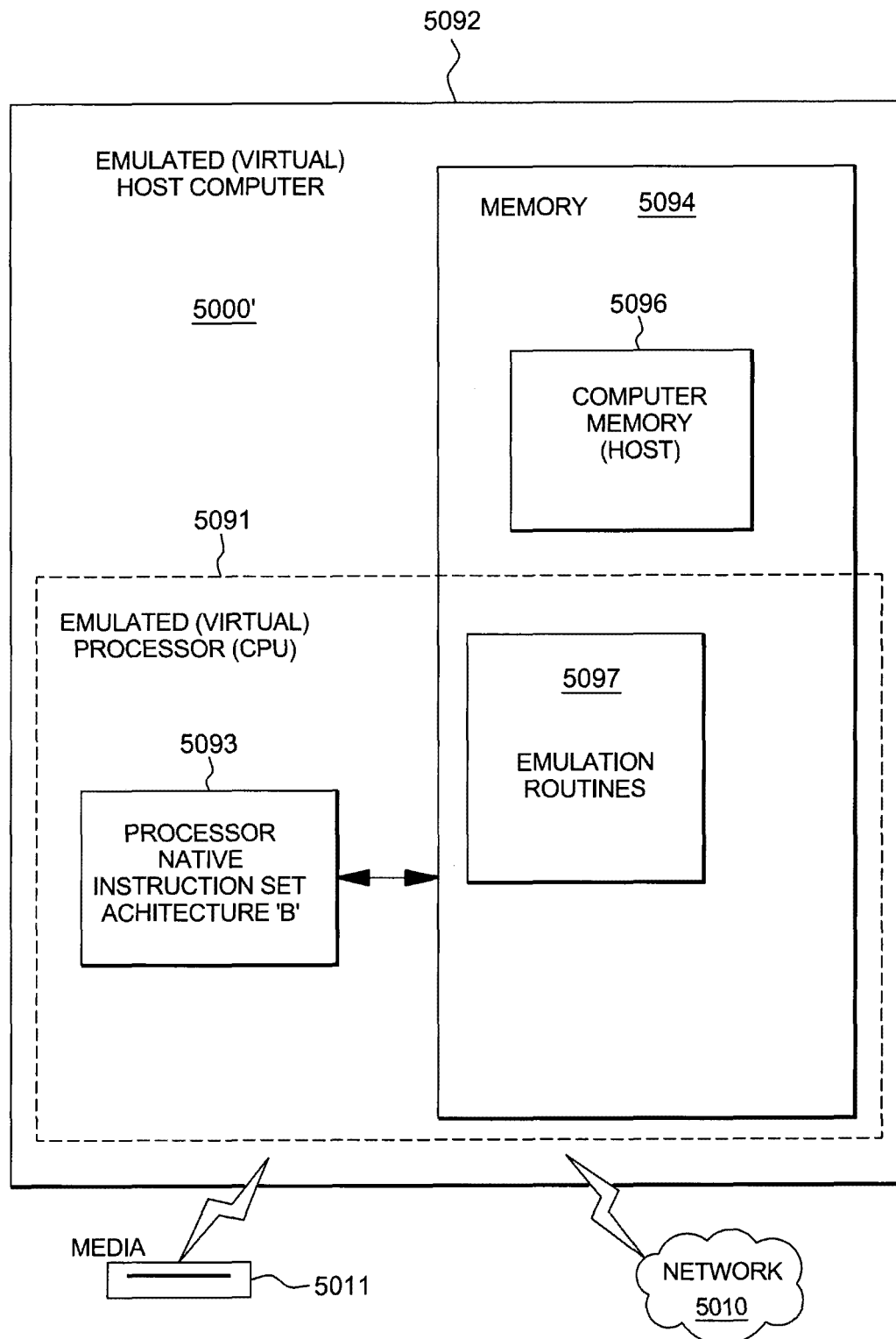


FIG. 16