

Integrated, three-dimensional cell configuration, integrated cooling array and cell-based integrated circuit**FIELD OF THE INVENTION**

The present invention relates to an integrated, three dimensional cell configuration. The present invention further relates to an integrated cooling array and a cell-based integrated circuit.

TECHNICAL BACKGROUND OF THE INVENTION

International patent application WO 03/060676 A2 describes a cooling system for a computer. The cooling system described therein comprises a cold side heat sink, a thermoelectric cooler (TEC) and a hot side heat sink which are arranged adjacent to each other and which are thermally coupled. Further, the cold side heat sink is arranged adjacent to a central processing unit (CPU) to be cooled. Here, the CPU forms the heat source. When power is supplied to the TEC, the STEC uses the Shifted and stitched Thermoelectric cooling effect to create a heat flux in order to transport and exhaust heat from the heat source at the CPU through the cold side heat sink and the STEC to the hot side heat sink where a fan is provided for pulling away heated air at the hot side heat sink.

A similar cooling system employing a thermoelectric unit for providing an active cooling of a CPU is described in international patent application WO 01/90866 A2. International patent application WO 2007/015701 describes thin-film thermoelectric devices for hot-spot thermal management in microprocessors. The thermoelectric cooling structure described therein is arranged on top of the chip. All above described thermoelectric cooling devices are in common that the cooling unit forms a separate unit which is not part of the structure to be cooled. The major problem of those cooling structures is that the effectiveness of cooling is comparably low since the heat generated by a corresponding heat source has to be transported always from the heat source to the thermoelectric cooling device. An alternative implementation of the Shifted and stitched Thermoelectric cooling is i.e. refrigerator, air conditioning and, or industrial cooling and, or heating system, due to its high coefficient of performance.

SUMMARY OF THE INVENTION

Hence, it is a challenge to improve a generic cooling system which already comprises a thermoelectric cooling device. In accordance with the present invention, a cell configuration having the features of claim 1 and/or an integrated cooling array having the features of claim 31 and/or a cell-based integrated circuit having the features of claim 33 is/are provided.

Accordingly, it is provided:

Integrated, three-dimensional cell configuration, comprising:
a semiconductor substrate or quartz substrate or sapphire or any other dielectric substrate (10); and
at least two arrays of thermoelectric cooling arrangement (120) mounted within and part of the quartz substrate or sapphire or any other dielectric substrate (10) for heat dissipation, the thermoelectric cooling arrangement (120) comprising:

- one first main region (1400) of a first conductivity type;
- at least one second main region (180); and
- at least one independently controllable thermoelectric cooling region (200) arranged between the first main region (1400) and the at least one second main region (180), wherein the at least one thermoelectric cooling region (200) comprises at least one Shifted and stitched Thermoelectric cooling element

and, or

at least one arrangement of embedded "Shifted and stitched Thermocouple elements" which is with via (470) to the top level of the mounted thermoelectric cooling arrangement compressing,

- at least one first main region (044) of a first or second conductivity type;
- at least one second main region (048); of a first or second conductivity type; and
- at least one thermoelectric cooling region (046) arranged between the first main region (044) and the at least one second main region (048), wherein the at least one thermoelectric cooling region (050) comprises at least one "shifted and stitched thermocouple element";

and, or

- at least one array of diode connected to the cooling arrangement (220) and at least one array of transistor (240) which triggers the thermoelectric cooling arrangement

and, or

- at least one arrangement of Seebeck elements of stitched thermoelectric cooling arrangement for cogeneration or generation of electricity on the top level of the mounted on shifted and stitched thermoelectric cooling arrangement or embedded in a substrate

and

at least one arrangement of embedded "Shifted and stitched Thermocouple elements" which is with via-temperature sensitive triggered conductive substrate (470) to the bottom level of the mounted thermoelectric cooling arrangement compressing,

- one first main region (140) of a first conductivity type;
- at least one second main region (180); and
- at least one independently controllable thermoelectric cooling region (200) arranged between the first main region (140) and the at least one second main region (180), wherein

the at least one thermoelectric cooling region (200) comprises at least one Shifted and stitched Thermoelectric cooling element(500)

and

- wherein the coefficient of performance of the thermoelectric cooling is at least 1.

- An integrated cooling array, comprising: a semiconductor substrate, a plurality of cell configurations according to the present invention wherein the cell configurations are arranged in an array within the commonly used semiconductor substrate.

- A cell-based integrated circuit, comprising: at least one cell configuration according to the present invention, a control device connected to each gate region for controlling the operation of each gate region independently.

The present invention is related to a three-dimensional thermoelectric cooling structure which overcomes the problems described with regard to known thermoelectric cooling devices employing separate cooling means. The present invention overcomes all known approaches by simply and effectively integrating the thermoelectric cooling structures within a semiconductor material. The basic idea of this invention is, therefore, to place the thermoelectric cooling structures directly in those areas and portions of the semiconductor substrate where the heat is generated. In known approaches the thermoelectric cooling structures are arranged directly nearby the semiconductor substrate in order to place the cooling structure in close proximity of the heat source. However, it is the finding of the present invention that it is still possible to arrange the thermoelectric cooling structures in even closer proximity to the heat source. The basic idea of the present invention, therefore, refers to an integrated, three-dimensional cell configuration where the thermoelectric cooling arrangement is integrated within the semiconductor material in close proximity to the corresponding heat sources. Employing such an integrated cell configuration reduces the distance between the area of the heat generation and the area of the thermoelectric cooling significantly and thus brings more efficiency to the whole cooling structure.

An integrated circuit comprises at least one thermoelectric cooling (TEC) arrangement, wherein the switches for triggering the at least one thermoelectric cooling region is also integrated within the substrate. Thus, it is possible to provide a more robust thermoelectric cooling device compared to prior art solutions. Moreover, the integrated circuit comprises at least one STEC arrangement that may be triggered with a given sequence to adjust the average current through the STEC region to a preferred value. This is a significant advantage compared to thermoelectric cooling devices according to the prior art which only allow a temperature control by supplying a certain power or voltage on both ends of the Shifted and stitched Thermoelectric cooling element.

One further advantage of the present invention is that within several only few micrometers a high temperature difference may be realized.

Further, this invention enables such as the implantation of thermoelectric cooling device for industrial cooling in machinery, cooling systems and freezing systems and due to its high Coefficient of Performance (COP) property which is at least 1.

Further, it is possible to increase the sensitivity and accuracy of semiconductor devices, such as (nano) sensors significantly. Last but not least, another main advantage is the possibility to provide smaller semiconductor devices. Further embodiments of the present invention are subject of the further subclaims and of the following description, referring to the drawings.

In a preferred embodiment the cell configuration has a three dimensional

cubic, rectangular, cylindrical, elliptical or spherical shape. However, it may also be possible and preferable that the cell configuration has a shape different of a cubic shape, such as a cylindrical shape, an elliptical shape or any other trench-like shape. Also combinations of them are possible. In a further very preferred embodiment the cell configuration has a spherical shape or spheric-like shape. Those configurations do not anymore have distinct corners, shifted and stitched and edges. Those shifted and stitched, edges and corners are rounded down which have the advantage that tunnelling between adjacent configurations will be reduced due to reduced capacities between those configurations.

In a further preferred embodiment the cell configuration has a cell size, wherein a cell size of the cell configuration is in the range from 160 nm to 400 nm, preferably in the range from 200 nm to 400 nm, preferably in the range from 100 nm to 200 nm, preferably in the range from 1000 nm to 100 nm preferably in the range from 500 nm to 1000 nm, preferably in the range from 030 nm to 500 nm, preferably in the range from 160 nm to 030 nm.

In a further preferred embodiment the cell configuration has a cell size below 160 nm and especially in the range between 1 nm - 120 nm and most preferably in the range between 5 nm - 80 nm and especially most preferably in the range between 100 nm - 030 nm.

In a further preferred embodiment the cell configuration further comprises further comprising at least one via region (490) which has the via function for controlling a carrier flow between the first main region (140) and the first main regions (044) wherein each via region (490) is electrically connected when the temperature is at the required level to a corresponding thermoelectric cooling region (200) and at least one via region (490) which has the via function for a carrier

flow between the second main region (180) and the second main regions (180) wherein each via region (490) is electrically connected.

In a further preferred embodiment the cell configuration further comprises wherein the at least one via region (490) is embedded within the dielectric substrate and wherein the number of thermoelectric cooling regions (200) corresponds to the number of via regions (490) and wherein each via region is directed to a corresponding thermoelectric cooling region (200).

In a further preferred embodiment the cell configuration further comprises wherein the cell configuration comprises a plurality of thermoelectric cooling regions (200), wherein each one of the plurality of thermoelectric cooling regions (200) employs the same first main region (140) but a different via region (490).

In a further preferred embodiment the cell configuration further comprises at least one gate region for controlling a carrier flow between the first and second main regions. Each gate region is electrically connected to a corresponding thermoelectric cooling region.

In a further preferred embodiment the cell configuration comprises at least one gate region which is embedded within the semiconductor substrate. The number of thermoelectric cooling regions corresponds to the number of gate regions wherein each gate region is directed to a corresponding thermoelectric cooling region. By employing different gate regions for each of the thermoelectric cooling regions it is possible to independently control these thermoelectric cooling regions based on corresponding demands or specified by the corresponding application.

In a further preferred embodiment the cell configuration comprises a plurality of thermoelectric cooling regions. Preferably, each of the plurality of thermoelectric cooling regions employs the same first main region but a different gate region. By using only one first main region it is possible to provide an area optimized layout of the whole cell configuration.

In a preferred embodiment the cell configuration comprises a plurality of thermoelectric cooling regions. Each of the plurality of thermoelectric cooling regions employs the same first main region, however, comprises a different gate region. The first main region may be a source region or a drain region. By having only one first main region it is possible to provide an area optimized structure of the cell configuration which comprises several switching elements which may be controlled independently from each other. With this arrangement it is possible to separately select one or more thermoelectric cooling arrangements within the same cell configuration by independently triggering the gate region.

In a preferred embodiment the thermoelectric cooling arrangement comprises a plurality of finger-like structures (480). These finger-like structures preferably extend from the first main region in a radial manner. Typically, but not necessarily, each finger-like structure may comprises one gate region, one thermoelectric cooling region and one second main region, which are typically arranged sequentially to each other.

In a further preferred embodiment the finger-like structures within the thermoelectric cooling arrangement are extending radially straight lined, i.e. linearly or straight forward. The whole arrangement then forms a star-like structure of the thermoelectric cooling arrangement.

In an alternative embodiment the finger-like structures are extending radially in a more or less dense package forming a meander, spiral or any other dense package structure wherein the finger-like structures are partially straight lined and/or curved.

In a further preferred embodiment the thermoelectric cooling arrangement comprises at least four, preferably at least six and more preferably especially at least eight radial extending finger-like structures.

In a further preferred embodiment the first main region comprises a surface area which has a rectangular and especially a quadratic shape. Especially in those configurations it is feasible and advantageous if the thermoelectric cooling arrangement comprises four or more finger-like structures. However, it may also be possible that the first main region has a hexagonal or octagon shape, whereas in those embodiments it is advantageous when the thermoelectric cooling arrangement comprises six finger-like structures in the case of a hexagonal-shaped of the first main region and eight finger-like structures in the case of an octagon-shaped first main region. Generally speaking it is advantageous, but not necessary, if the amount of finger-like structures depends on the amount of borderlines or edges of the first main region. However, it may also be possible, that the surface area of the first main region has a round shape, especially an elliptical, circular or oval shape. These embodiments have the advantage that there are no distinct edges at the borderlines of the first main area which is in terms of electric fields and in order to prevent tunneling most effective and advantageous. In a first typical embodiment the first main region is designed to form a source region and the second main regions are then designed to form corresponding drain regions. In an alternative embodiment, the first main region is designed to form a drain region. Then, the second main regions are designed to form corresponding source regions. The first main region and the second main regions are typically, but not necessarily, of the same conductivity type. For example the first main region and

second main regions are of a p-type semiconductor material. Alternatively, the first main region and the second main regions may also be of an n-type semiconductor material. Depending on the structure of the cooling regions, especially if the cooling region comprises an uneven number of STEC -elements, the first main region is of a first conductivity type, whereas the second main region is of a second conductivity type different than the first conductivity type. In a further preferred embodiment at least one of the Shifted and stitched Thermoelectric cooling elements of the thermoelectric cooling arrangements comprises a first subregion of a third conductivity type and a second subregion of a fourth conductivity type. The third and fourth conductivity types are different from each other. For example the third conductivity type is an n-type or p-type semiconductor material and the fourth conductivity type is a p-type or n-type semiconductor material, respectively. Both, the first and second subregions are spaced from each other in the horizontal direction.

In a preferred embodiment at least one of the thermoelectric cooling regions comprises a plurality of Shifted and stitched Thermoelectric cooling elements. Those pluralities of Shifted and stitched Thermoelectric cooling elements are sequentially arranged and connected to each other. Further, the plurality of Shifted and stitched Thermoelectric cooling elements may be arranged and connected in a mutually spaced manner such that always one first subregion is arranged adjacent to a second subregion and vice versa. With this configuration one Shifted and stitched Thermoelectric cooling element is arranged and connected adjacent to a second Shifted and stitched Thermoelectric cooling element and so on.

In a further preferred embodiment an interspace is provided between corresponding mutually spaced first and second subregions. The interspace is typically filled at least partially with an insulating material. The insulating material may be silicon dioxide, especially thermally grown silicon dioxide (SiO₂), PVD silicon dioxide, Low-K, High-K, silicon nitride, Hafnium Oxide or any other insulating material which need not necessarily be a semiconductor based material. It is especially preferred if the insulating material is Al₂O₃ and/or AgO or AuO or CuO since these materials have superior insulation proportions especially at the operation temperatures of the TEC.

In one preferred embodiment first and second subregions of a STEC -element or of adjacent STEC -elements have the same distance in the vertical projection. That means that these first and second subregions are equally distanced to each other in the vertical direction. In another very preferred embodiment, the plurality of STEC -elements within a thermoelectric cooling region are arranged in a zig-zag or staggered-like manner to each other such that the first and/or

second subregions are arranged shifted and stitched part in the vertical direction. This means, that a distance in the vertical direction between the first and second subregions is increasing or decreasing, respectively. In a further preferred embodiment a shifted and stitched of the first and/or second subregions referring to the horizontal plane is in the range between 5° and 85° . Especially the shifted and stitched is in the range between 45° and 60° , preferably in the range between 30° and 40° and most preferably in the range between 10° and 20° . It is a finding of the present invention that depending on this shifted and stitched it is possible to achieve a higher temperature gradient between the hot side and cold side of the thermoelectric cooling arrangement and thus a better cooling. Additionally or alternatively, it is possible to provide lower trigger energy by providing a higher shifted and stitched.

In a further preferred embodiment the first and/or second subregions of a thermoelectric cooling region or a Shifted and stitched Thermoelectric cooling element have a multipart structure, especially a two-part structure. This multipart structure has, according to a further embodiment, a first part having a first shifted and stitched part and a second part having a second shifted and stitched part. The first part is typically in direct contact with the bridge contact member. The second part is in contact with the first part and may be in contact with a bridge contact member of an adjacent Shifted and stitched Thermoelectric cooling element. Preferably, but not necessarily, the first shifted and stitched is lower than the second shifted and stitched part. Especially the first shifted and stitched part is in the range between 15° and 45° and especially in the range between 25° and 35° . The second shifted and stitched is then in the range between 45° and 85° and especially in the range between 60° and 70° .

Preferably each of the first and second subregions comprises two boundary interfaces. The boundary interfaces of adjacent and mutually spaced first and second subregions are connected via bridge contact members. Those bridge contact members of mutually spaced first and second subregions are arranged preferably in a staggered manner. In a preferred embodiment a first bridge contact member extends from a first boundary interface of the first subregion to a second boundary interface of the second subregion in order to electrically connect corresponding mutually spaced first and second subregions with each other. In a very preferred embodiment the bridge contact members comprise an electrically very high conductive material, such as highly doped polysilicon, metal or an electrically high conductive alloy. Typical materials for the bridge contact members are therefore aluminium, gold, silver, wolfram, titan, etc. or alloys thereof. In a further preferred embodiment at least one electrical shield layer is

provided. This electrical shield layer is arranged adjacent to a hot side of a thermoelectric cooling region. The shield layer is adapted to provide a high thermal conductivity from the semi-conductor substrate to the hot side of the thermoelectric cooling region. This shield layer is further adapted to prevent an electrical connection between the semiconductor substrate to the hot side of the thermoelectric cooling region. Consequently, this shield layer covers the thermoelectric cooling region and is arranged on top or below the corresponding bridge contact members. These shield layers are therefore designed to electrically protect the Shifted and stitched Thermoelectric cooling elements and to provide a thermally high conductivity for providing optimal heat conduction from the hot side of the thermoelectric cooling region.

Typically, but not necessarily two Shifted and stitched Thermoelectric cooling elements of the same thermoelectric cooling regions are arranged adjacent to each other and are connected via a second bridge contact member. This second bridge structure extends typically from a third boundary interface of the second subregion of a first Shifted and stitched Thermoelectric cooling element to a fourth boundary interface of the first subregion of a second Shifted and stitched Thermoelectric cooling element. Having this arrangement of the bridge contact elements bridging subregions of adjacent Shifted and stitched Thermoelectric cooling elements it is possible to provide a thermoelectric cooling region in a staggered manner.

In a preferred embodiment the adhesion of the regions and parts on the dielectric substrate are embedded with an adhesion layer (410) and which can be used/is as a substrate layer with thermal conductivity properties.

In a preferred embodiment the regions comprising: wherein at least one layer of thin film substrate of the bridge compresses an alloy of a metal with Nitrogen whereby the range of the Nitrogen is between 0,01% to 50% atomic weight of the alloy such as, TiN; TiN_{0,5}; AlN; AlN_{0,1}

and, or a combination of multiple layers of thin film substrate with

an alloy, with high-k or low-k property.

In a further preferred embodiment the integrated cooling array, comprising:

At least one layer of thin film semiconductor substrate doped with Nitrogen, and, or Boron and, or Selenium, a plurality of cell configurations according to any of the claims 1 to 36, wherein the cell configurations are arranged in an array within the commonly used semiconductor substrate.

In a further preferred embodiment Integrated cooling array, comprising:

At least one layer of thin layer semiconductor substrate doped with Nitrogen, and, or Boron and, or Selenium and, or a

plurality of cell configurations according array wherein the cell configurations are arranged in an array compressing within the commonly used semiconductor substrate.

In a further preferred embodiment the Integrated cooling array compressing:

wherein the first shifted and stitched part (700) is in the length of the first subregion (030) between $1/99$ and $47/500$ of the first part, especially in the length of the first subregion (030) between $1/4$ and $1/3$ of the first part, or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the first part and/or wherein the second shifted and stitched part (710) is in the length of the second subregion (032) between $1/99$ and $47/500$ of the second part, especially in the length of the first subregion (030) between $1/4$ and $1/3$ of the second part, or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the second part, and/or wherein the third shifted and stitched part (720) is in the length of the first subregion (030a) between $1/99$ and $47/500$ of the third part, especially in the length of the first subregion (030a) between $1/4$ and $1/3$ of the third part, or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the third part, and/or

wherein the fourth shifted and stitched part (730) is in the length of the first subregion (030b) between $1/99$ and $47/500$ of the fourth part, especially in the length of the first subregion (030b) between $1/4$ and $1/3$ of the fourth part or especially in the length of the second subregion (032b) between $1/5$ and $1/4$ of the fourth part.

In a further preferred embodiment, Integrated cooling array, comprising:

wherein each of the first and second subregions (030, 032) comprise two boundary interfaces (038, 040), wherein the boundary interfaces (038, 40) of adjacent and mutually spaced first and second subregions (030, 032) are connected via bridge contact members (036, 420).

In a very preferred embodiment the shield layers comprise a thermally high conductive and electrical isolating material. Such a high conductive isolating material may be advantageously almost with synthetic diamond. In a very preferred embodiment the synthetic diamonds are thermally grown and embedded within the substrate. This allows a decrease of the diameters of the first and second subregions perpendicular to the direction of the current compared to a corresponding subregion formed of a metal. Other materials which at least provide good isolation are silicon oxide, low-K, high-K and the like. By suitably doping those materials it is possible to provide also a good thermal conductivity.

In a further preferred embodiment at least one cooling layer is provided. This cooling layer contacts the bridge contact member at a cold side of the thermoelectric cooling region.

Preferably, this cooling layer comprises a high thermal conductivity in order to dissipate heat from the thermoelectric cooling region. Preferable materials for these cooling layers are synthetic diamond.

In a further preferred embodiment of the cooling array the cell configurations are electrically connected in serial connection to each other. Alternatively, it may also be possible that the cell configurations are arranged in a parallel connection to each other. It goes without saying that also combinations of those electrical connection types may be possible such as partial serial and partial parallel connections.

In a further preferred embodiment the control device comprises a program controllable device having a frequency clock generator and a counter which is triggered by the clock generator. The gate regions of each cell configurations are triggered by the counter according to the counter readings.

In a further preferred embodiment the gate regions of each of the cell configurations are triggered either in a serial or in array.

In a further preferred embodiment of the integrated circuit device regions are defined between adjacent cooling arrangements of the same cell configuration or of adjacent cell configurations. In an additional or alternative embodiment the device regions are arranged at a cold side or hot side of the thermoelectric cooling arrangements. The integrated circuit further comprises at least one semiconductor device which is arranged in one of the device regions of the integrated circuit between adjacent thermoelectric cooling arrangements. This allows a very compact and area optimized arrangement of the cell configuration on the one hand and the semiconductor devices on the other hand. Areas within the cell configurations which are not used for thermoelectric cooling may, therefore, preferably be used for other semiconductor devices, for example for such semiconductor devices which show a high heat emission. The heat which is produced by these semiconductor devices may then be efficiently transported by their cell configuration and especially by the thermoelectric cooling arrangements within the cell configurations.

In some preferred embodiments the semiconductor device may be at least one of the following: A sensor, especially a heat sensor, an optical sensor, a thermal sensor or the like.

A rectifier element, such as a diode, a Wheatstone bridge, or any other bridge structure. A switching element, especially a transistor. The transistor may be a MOSFET, such as a NMOS, PMOS, VMOS, a power-MOSFET, a JFET, a bipolar transistor, an IGFET, an IGBT or any other semiconductor transistor. A control element. A programmable device, especially a microprocessor, a microcontroller, a programmable logic device, such as a FPGA or PLD, a memory device, such as a

DRAM, SRAM, ROM, PROM or the like. A solar cell, a laser diode, a LED, a micro strip and alike. However, it should be noted that those semiconductor devices are nearly examples and the present invention should not be restricted to these embodiments.

In a further preferred embodiment the semiconductor device is spaced from the first main regions and the thermoelectric cooling arrangements. Additionally the semiconductor device may be arranged between at least two of the thermoelectric cooling arrangements.

In a further preferred embodiment, referring to the first main region, the semiconductor device is arranged within a radius in a range of 1 nm - 100 μ m from a center of the first main region, preferably in the range between 500 nm and 1 μ m.

In a preferred embodiment of the integrated circuit device, the first main region is surrounded by at least two radial extending domains, each domain comprising one gate region, one second main region and one thermoelectric cooling region.

Thus, it is possible to use a single first main region for connecting several gate regions and thermoelectric cooling regions to an energy source. Due to the increased usability of the first main region in this embodiment, it is possible to decrease the volume necessary to realise a triggerable STEC region without decreasing the size and/or volume of the STEC region itself.

In another preferred embodiment the integrated circuit comprises a counter with a clock signal creator connected to a power supply, wherein the at least one gate region is connected to the counter via at least one conducting element. The triggering of the at least one STEC region is thus easily performable.

In another preferred embodiment the integrated circuit is designed such in order to be operable with a current in the range of 0,5 pA and 500 mA, especially in the range 1 mA and 200 mA, preferably in the range of 1 pA and 100 μ A, and most preferably in the range between 100 pA and 1 μ A.

In another preferred embodiment of the cell configuration a plurality of controllable thermoelectric cooling region are provided. At least two of the controllable thermoelectric cooling region and especially a plurality of the controllable thermoelectric cooling region have different shifted and stitches.

In another preferred embodiment a plurality of thermoelectric cooling regions are provided wherein the plurality of thermoelectric cooling regions are extending in a star-like manner outwards from the first main region. In an especially preferred each of the star-like extending thermoelectric cooling regions is triggerable independently.

In another preferred embodiment the thermoelectric cooling arrangement is operable to code digital data by independently

triggering the thermoelectric cooling regions having different shifted and stitched s.

In another preferred embodiment the thermoelectric cooling arrangement is operable as a temperature sensor by independently triggering the thermoelectric cooling regions having different STEC.

In a preferred embodiment at least two thermoelectric cooling arrangements are stacked within the semiconductor substrate one upon the other.

In a preferred embodiment an interlayer is provided between adjacently arranged thermoelectric cooling arrangements wherein the interlayer is defining a distance between two adjacent thermoelectric cooling arrangements.

In a preferred embodiment the distance is at least 5 nm and most preferably between 5 nm and 120 nm.

In a preferred embodiment the interlayer comprises at least partially and preferably completely an isolating material.

In a preferred embodiment at least one connecting device is provided. The connecting device is arranged between at least two thermoelectric cooling arrangements and preferably between two stacked and/or adjacently arranged thermoelectric cooling arrangements. The connecting device comprises a thermally high conductive and electrically isolating material in order to provide a thermal connection between the two thermoelectric cooling arrangements and further to guarantee an electrical isolation between the two thermoelectric cooling arrangements.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings. The invention is explained in more detail below using exemplary embodiments which are specified in the schematic figures of the drawings, in which:

Fig. 1 shows a cross section view of a first, basic embodiment of a cell configuration according to the present invention;

Fig. 2 shows by means of a cross section a section of a thermoelectric cooling region for an integrated circuit device such as shown in Fig. 1;

Fig. 2A-2D show cross sections of different Shifted and stitched Thermoelectric cooling elements of a STEC region according to the present invention;

Fig. 3 shows a plan view of a second embodiment of a cell configuration according to the present invention.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily drawn to scale. For example, the chosen elements are only used to help to improve the understanding of the functionality and the arrangements of these elements in various embodiments of the present invention. Also, common but

well understood elements that are useful or necessary in a commercial feasible embodiment are mostly not depicted in order to facilitate a less abstracted view of these various embodiments of the present invention. It will further be appreciated that certain actions and/or steps in the described methods may be described or depicted in a particular order of occurrences while those skilled in the art will understand that such specificity with respect to sequence is not actually required. Skilled person will appreciate that the embodiment of this invention is not be illustrated due to its simplicity and clarity in the description. It will also be understood that the terms and expressions used in the present specification have the ordinary meaning as it accorded to such terms and expressions with respect to their corresponding respective areas of inquiry and study except where specific meanings have otherwise be set forth herein.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE PRESENT INVENTION
Hereinafter, before describing the present invention we want to briefly discuss some general aspects of the invention. The present invention is directed generally to thermoelectric cooling. Although commercial thermoelectric cooling modules were not available until almost 1960, the basic physical principles upon which modern thermoelectric coolers are based on actually date back to early 1800s. In the early 1800s Thomas Seebeck discovered that an electric current would flow continuously in a closed circuit made up of two dissimilar metals, provided that the junction of the metals were maintained at two different temperatures. This is also known as the Seebeck effect.

The thermoelectric effect is the direct conversion of temperature differences to electric voltage and vice versa. A thermoelectric device creates a voltage when there is a different temperature on each side. Conversely when a voltage is applied to it, it creates a temperature difference, also known as the Shifted and stitched Thermoelectric cooling effect. At atomic scale an applied temperature gradient causes charged carriers in the material whether they are electrons or electrons holes, to diffuse from the hot side to the cold side. This causes the so-called thermally induced current. This effect can be advantageously used to generate electricity, to measure temperature, to cool or heat objects, etc. Since the direction of heating and cooling is determined by the sign of the applied voltage, thermoelectric devices make very convenient temperature controllers.

Traditionally, the term "thermoelectric effect" or "thermoelectricity" encompasses three separately identified effects, the Seebeck effect, the Shifted and stitched Thermoelectric cooling effect and the so-called Thomseffect. In many textbooks and prior art documents, the thermoelectric effect may also be called the STEC -Seebeck effect. The

Seebeck effect is the conversion of temperature differences directly into electricity. The Shifted and stitched Thermoelectric cooling effect, however, is the reversal of the Seebeck effect. When a current is made to flow through a circuit of two different metals heat is evolved at the upper junction and absorbed at the lower junction which leads to a heat transfer from the hot side to the cold side. The present invention addresses a so-called Shifted and stitched Thermoelectric cooling element which can be either used for the Shifted and stitched Thermoelectric cooling effect and thus for a heat transfer as well for the Seebeck effect to generate electricity due to a heat gradient. In case of using the Shifted and stitched Thermoelectric cooling effect, hereinafter Shifted and stitched Thermoelectric cooling is also called "Shifted and stitched thermoelectric cooling" or shortly "STEC".

Thus, the Shifted and stitched Thermoelectric cooling element is just an opposite phenomenon of the Seebeck effect, whereby the thermal energy could be absorbed at one different metal junction and discharged at the other junction when an electric current is flowing within the closed circuit. Since the basics of the Seebeck effect and Shifted and stitched Thermoelectric cooling effect are well known these physical effects are not described in more detail. With regard to the principals of the thermoelectric cooling the document MPE6350: "Electronics Cooling", of the Cairo University, Faculty of Engineering, especially Chapter 17, is herewith incorporated fully by reference.

Hereinafter, the present invention is described in more detail with regard to the embodiments in the drawings.

Fig. 1 shows a sectional view of a first, basic embodiment of a cell configuration according to the present invention. The cell configuration is denoted by reference number 100. The cell configuration 100 comprises a substrate 110 having a first top surface 110a and a second bottom surface 110b. The substrate 110 may be a doped semiconductor substrate, for example a doped silicon substrate. However, the present invention is not restricted to a substrate 110 formed of silicon but can also be any other semiconductor material, such as GaAs, SiC and the like or any other dielectric substrate such as quartz, sapphire.

In Fig. 1 the cell configuration 100 comprises one thermoelectric cooling arrangement 120 which is arranged within the semiconductor substrate 110. This thermoelectric cooling arrangement 120 is used for heat dissipation, for example for heat dissipation of any integrated circuit within the same semiconductor substrate. Therefore, this thermoelectric cooling arrangement 120 is, according to a basic idea of the present invention, an integrated part of the semiconductor substrate 110.

The thermoelectric cooling arrangement 120 comprises one first main region 140, two second main regions 180 and two thermoelectric cooling STEC regions 200. The first main region 140 is arranged centrally within the thermoelectric cooling arrangement 120 and is of a first conductivity type, for example n-type or p-type. Depending on the structure of the thermoelectric cooling regions 200 the two second main regions 180 may be of a first conductivity type or of a second conductivity type different than the first conductivity type. The two second main regions 180 are electrically coupled with the first main region 140 through corresponding thermoelectric cooling regions 200 which are arranged between the first centrally arranged main region 140 and the two second marginally arranged main regions 180.

In the present case the first main region 140 may be a source or a drain region, whereas the second main region 180 then forms the drain or the source region, respectively. Hence, the thermoelectric cooling arrangement 120 forms two controllable switches, especially transistors, whereas the control terminals are formed by corresponding gate regions 160. These gate regions 160 are arranged within the thermoelectric cooling regions 200 and are preferably arranged directly adjacent to the first main region 140. Having this structure of the thermoelectric cooling arrangement 120 both transistors and thus the functionality of both thermoelectric cooling regions 200 can be controlled independently.

The essential feature is here that each of the thermoelectric cooling regions 200 comprises at least one Shifted and stitched Thermoelectric cooling element. The detailed structure and functionality of the thermoelectric cooling arrangement 120 and the Shifted and stitched Thermoelectric cooling elements therein is hereinafter described in more detail with regard to several embodiments shown in Fig. 2A-2D. The first main region 140, the second main regions 180, the gate region 160 and the semi electric cooling regions 200 are in the present embodiment embedded within the substrate L. However, these regions may also be arranged adjacent to the top or bottom surfaces 110a, 110b of the substrate 110.

In one advantageous embodiment the integrated circuit device comprises at least a first STEC arrangement 120 and a second STEC arrangement 120. In this case, the radial extending domains of two adjacent STEC arrangements 120 are distant and non-overlapping. The first STEC arrangement 120 may be formed different than the second STEC arrangement 120. For instance, the first STEC arrangement 120 may have a thickness of a gate oxide, a length of a channel region, an inner shifted and stitched, a number of radial extending domains, a thickness of the at least one second main region 180, a dopant concentration and/or a dopant type that differ from the corresponding parameters of the second STEC arrangement 120.

Alternatively, the integrated circuit device 100 may also comprise at least two STEC arrangements 120 with identical parameters.

In case, that the integrated circuit device 100 comprises a plurality of STEC arrangements 120 several of these STEC arrangements 120 may be connected with each other to build a controllable three dimensional STEC device. For instance, the at least two STEC arrangements 120 may be electrically connected and triggered in series to each other. However, the integrated circuit device 120 is not restricted to such an electrical connection between different STEC arrangements 12. The at least two STEC arrangements 120 may also be electrically connected and triggered in parallel to each other. Furthermore, the at least two STEC arrangements 120 may be triggered serial or parallel at the same time such that a tongue shaped cooling area within the first layer material covered by the second layer material is generated. The tongue shape may be increased, when the electrical current is adjusted accordingly. Thus, the second layer material may be used for recreation of a heat gradient or the region of the first layer material may be a heat sink.

The surrounding of the STEC arrangement 120 is cooled down when an electrical current has been triggered by the gate region through the STEC regions 200. Therefore, a heat source embedded within the substrate 100 may be compensated using the inventive technique. The at least one heat source may be an external or internal heat source. For instance, the at least one heat source may be also embedded within the substrate 100. Moreover, the at least one heat source may also be arranged within the surrounding of the at least one STEC arrangement 12. Preferable, the at least one heat source is arranged in a distance around a middle point of the first main region 140. Thus, the cooling function of the STEC arrangements 120 ensures that no damage occurs due to heat produced by the heat source occurs.

The at least one heat source may be a sensor, a diode or any other heat producing device. The inventive technique can therefore be used to improve a detecting capacity of several sensors arranged in the surrounding of a STEC arrangement 120. Thus, localized signals can be detected accurately. Moreover, the sensor and / or diode may be connected as an input or output to the device. The diode may be an infrared photodiode, an X-ray photodiode and/or a laser-diode. Specially, the photodiode may be cooled as a wave shape, which propagates towards the edge of the second main region 18. Thus, the inventive technique can also be used for an energy recovery. Fig. 2 shows a cross section of a detail of the integrated circuit device of Fig. 1 in the area of the STEC region. The cross section runs through a STEC region 200 parallel to its longitudinal axis.

The STEC region 200 shown in Fig. 2 comprises several Shifted and stitched Thermoelectric cooling elements 500. Each Shifted and stitched Thermoelectric cooling element 500 comprises a first subregion 030 of a third conductivity type and a second subregion 032 of a fourth conductivity type different than the third conductivity type. For instance, the first subregion 030 may be of the p-type, wherein the second subregion 032 is of the n-type. However, the STEC arrangement 120 is not restricted to such a Shifted and stitched Thermoelectric cooling element 50. In case that the first subregion 030 is of the n-type, the second subregion 032 is then of the p-type.

A Shifted and stitched Thermoelectric cooling element 500 also comprises a first insulating material that fills an interspace 340 between the first subregion 030 and the second subregion 032 at least partially. Preferably, the first insulating material fills the interspace between the first subregion 030 and the second subregion 032 completely. Moreover, a Shifted and stitched Thermoelectric cooling element 500 further comprises a first bridge contact member 036. The first contact member 036 extends from a first interface 380 of the first subregion 030 to a second interface 400 of the second subregion 032. The first interface 380 of the first subregion 030 and the second interface 400 of the second subregion 032 may both be directed towards one surface 110a, 110b of the substrate 110. Preferably, the first interface 380 and the second interface 400 are both extending parallel to the longitudinal axis 200a of the STEC region 200. However, the STEC arrangement 120 is not restricted to such a design of the subregions 030, 032, the interfaces 380, 400 and/or the first

bridge contact member 036.

In a preferred embodiment the STEC region 200 comprises at least two Shifted and stitched Thermoelectric cooling elements and most preferably a plurality of Shifted and stitched Thermoelectric cooling elements, each having the subregions 030, 032 and interspace 340. The STEC region 200 is not restricted to a certain number of such Shifted and stitched Thermoelectric cooling elements 500. Preferably, two adjacent Shifted and stitched Thermoelectric cooling elements 500, 500' of the same STEC region 200 are connected via a second bridge contact member 420, as it is shown in Fig. 2. The STEC region 200 may also comprise an insulating material 480 that fills the interspace 340 between subregion 030, 032 of the adjacent

Shifted and stitched Thermoelectric cooling elements 500' at least partially and especially completely.

The second contact subregion 420 may expand from a third interface 440 of the second subregion 032 of the first Shifted and stitched Thermoelectric cooling element 500 to a forth interface 460 of the first subregion 030 of the second

Shifted and stitched Thermoelectric cooling element 500'. The first Shifted and stitched Thermoelectric cooling element 500 is closer to the first main region 140 than the second Shifted and stitched Thermoelectric cooling element 500'. The third interface 440 of the second subregion 032 and the fourth interface 460 of the first subregion 030 may both be directed towards different surfaces 110a, 110b of the substrate 100 and/or extend parallel to the longitudinal axis 200a of the STEC region 200. Moreover, the third interface 440 and the fourth interface 460 may run parallel to the first interface 380 and the second interface 400.

The first bridge contact 036 member and/or the second bridge contact member 420 may comprise an electrical conducting material such as aluminium, gold, silver, etc. Thus, a good electrical conductivity between the different subregions 030, 032 of the Shifted and stitched Thermoelectric cooling elements 500, 500' of the same STEC region 200 is provided. The interfaces 380, 400, 440, 460 between the subregions 030, 032 and the bridge contact members 036, 420 are suited for the Shifted and stitched Thermoelectric cooling effect.

The STEC region 200 may be linked to the first main region 140, the gate region 160 and/or the second main region 180 via at least one bridge contact member 036, 420. Thus, a good electrical contact between the STEC region 200 and the adjacent first main region 140, gate region 160 and/or second main region 180 is provided.

In a preferred Cell configuration embodiment wherein the first shifted and stitched part (080) is in the length of the first subregion (030) between $1/99$ and $47/500$ of the first part, especially in the length of the first subregion (030) between $1/4$ and $1/3$ of the first part, or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the first part and/or wherein the second shifted and stitched part (080) is in the

length of the first subregion (030) between $1/99$ and $47/500$ of the second part, especially in the length of the first subregion (030) between $1/4$ and $1/3$ of the second part, or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the second part, and/or

wherein the third shifted and stitched part (080) is in the length of the first subregion (030) between $1/99$ and $47/500$ of the third part, especially in the length of the first subregion (030) between $1/4$ and $1/3$ of the third part, or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the third part, and/or

wherein the fourth shifted and stitched part (080) is in the length of the first subregion (030) between $1/99$ and $47/500$ of the fourth part, especially in the length of the first subregion (030) between $1/4$ and $1/3$ of the fourth part or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the fourth part.

In a preferred Cell configuration embodiment wherein the height of the thin film 750) of the subregions (030) and, or (032) is height range between $1/19$ and $4/5$ of the length of the first shifted and stitched part and, or second shifted and stitched part and, or third shifted and stitched part or fourth shifted and stitched part.

The STEC region 200 shown in Fig. 2 provides a thermal flux in a direction perpendicular to the longitudinal axis 200a, when a current is passing through the interfaces 380, 400, 440 and 460 and thus through the sequentially arranged Shifted and stitched Thermoelectric cooling elements. Thus, a thermoelectric cooling structure is provided, which enables a very high thermoelectric cooling capacity.

The STEC region 200 shown in Fig. 2 can be produced by standard semiconductor technology methods. Therefore, no description of a method to manufacture the different subunits 030, 032, 036, 420 is given herein.

Fig. 2A-2E show cross sections of different embodiments of a Shifted and stitched Thermoelectric cooling element within a STEC region. In the cross sections of different embodiments of a cut away of a thermoelectric cooling region which shows the structure of different Shifted and stitched Thermoelectric cooling elements.

In Fig. 2A, the Shifted and stitched Thermoelectric cooling element 500 comprises a first and second subregion 030, 032 which are interconnected to each other via a bridge contact member 036. In the embodiment of Fig. 2A the first and second subregions 030, 032 are arranged more or less vertically and orthogonal to the bridge contact member 036.

However, it is more advantageous that the first subregions 030, 032 are angled and thus having a horizontal orientation. This is shown with regard to the second embodiment of a thermoelectric cooling region 200 in Fig. 2B, where an shifted and stitched α is present between the subregions and the horizontal plane. Preferably, this shifted and stitched α is between 5° and 75° , preferably in the range between 15° and 25° and more preferably in the range between 25° and 35° .

Fig. 2C shows another embodiment of a Shifted and stitched Thermoelectric cooling element 500 of a thermoelectric cooling region 200. According to Fig. 2C the first subregion 030 comprises a first portion and a second portion and the second subregion also comprises a first portion 30a and a second portion 30b, which are connected to each other. Both of these portions of a corresponding subregion 030 are angled with regard to the horizontal direction x and z. However, a shifted and stitched β of the first lower portion 030a with regard to the horizontal direction is higher than an shifted and stitched β of the second upper portion 030b with regard to the horizontal direction x. This separation of the first and second subregions 030, 032 into two different portions 030a, 030b, 032a, 032b having different shifted and

stitches β , $\square$ is very advantageous for the electric and thermal properties of the thermoelectric cooling region 200. Especially, it has been shown that the whole thermoelectric cooling region 200 has a much better efficiency with this arrangement. Preferably the first shifted and stitched β is in the range up to 30° and the second shifted and stitched $\square$ is then in the range between 30° and 60° .

Fig. 2D shows a fourth, very preferred embodiment of the thermoelectric cooling region. In contrast to the embodiment of Fig. 2C, where the first and second shifted and stitched $\square$, $\square$ of the thermoelectric cooling region are identical for either the first and second subregions 030, 032, these shifted and stitched s are now different. For the first subregion 030 a

first shifted and stitched $\square_1$ of the first portion 030a and a second shifted and stitched $\square_1$ of the second portion 030b are typically different to the corresponding shifted and stitches $\square_2$, $\square_2$ of the first and second portions 032a, 032b of the second subregion 032. For example the shifted and stitched $\square_1$ of a second portion 030b of the first subregion 030 is 47° and the shifted and stitched $\square_2$ of a corresponding second portion 032b of the second subregion 032 is 42° .

The main advantage for providing shifted and stitched part first and second subregions 030, 032 of the Shifted and stitched Thermoelectric cooling elements 500 is the fact, that adjacent Shifted and stitched Thermoelectric cooling structures always have a minimum distance at the boundary interfaces and a maximum distance where there is no boundary interfaces between first and adjacent second subregions 030, 032. In terms of electrical coupling this is most effective. The bridge contact members 036 of a Shifted and stitched Thermoelectric cooling element 500 comprises an electrically high conductive material, such as aluminium, wolfram, tungsten or an alloy of these materials.

Between the bridge contact members 036 and the semiconductor substrate 110 typically a coating or shield layer is provided. Preferably, the coating or shield layer is only necessary on the hot side of the Shifted and stitched Thermoelectric cooling element 500 or the thermoelectric cooling regions. However, it may also be possible to provide such coating layers on the cold side of the thermoelectric cooling region since the whole thermoelectric cooling arrangement 120 may also be used in both directions where the cold side may form the hot side and vice versa. The coating layer may comprise any material which is thermally highly conductive in order to provide a high effective heat transfer from the hot side of the semiconductor substrate through the coating layer to the thermoelectric cooling region. Such material for the coating layer may be synthetic diamond.

The invention is not restricted to a certain number of such Shifted and stitched Thermoelectric cooling elements 500. Fig. 2E A shows a cross section of a STEC region 200 comprising a plurality of Shifted and stitched Thermoelectric cooling elements 500. Each Shifted and stitched Thermoelectric cooling element 500 comprises a first and second region 030, 032 and an interspace 340 between adjacent first and second regions 030, 032. Preferably, two adjacent Shifted and stitched Thermoelectric cooling elements 500, 500' of the same STEC region 200 are connected via a second bridge contact member 420, as this is shown in Fig. 3A. The STEC region 200 comprises an insulating material 480 that fills the interspace 340 between the first and second regions 030, 032 of adjacent Shifted and stitched Thermoelectric cooling elements 500' at least partially and especially completely.

The second contact region 420 may expand from a third interface 440 of the second region 032 of the first Shifted and stitched Thermoelectric cooling element 500 to a forth interface 460 of the first region 030 of the second Shifted and stitched Thermoelectric cooling element 500'. The first Shifted and stitched Thermoelectric cooling element 500 is closer to the first main region 140 than the second Shifted and stitched Thermoelectric cooling element 500'. The third interface 440 of the second region 032 and the forth interface 460 of the first region 030 may both be directed towards different surfaces 110a, 110b of the substrate 100 and/or extend parallel to the longitudinal axis 200a of the STEC region 200. Moreover, the third interface 440 and the forth interface 460 may run parallel to the first interface 380 and the second interface 400.

The first bridge contact 036 member and/or the second bridge contact member 420 comprise an electrical conducting material such as aluminium, gold, silver, etc. or an alloy comprising at least one of these materials. Thus, a good electrical conductivity and also a pretty good thermal conductivity between the different regions 030, 032 of the Shifted and stitched Thermoelectric cooling elements 500, 500' of the same STEC region 200 is provided. The interfaces 380, 400, 440, 460 between the regions 030, 032 and the bridge contact members 036, 420 are suited for the Shifted and stitched Thermoelectric cooling effect.

The STEC region 200 may be linked to the first main region 140, the gate region 160 and/or the second main region 180 via at least one bridge contact member 036, 420. Thus, a good electrical contact between the STEC region 200 and the adjacent first main region 140, gate region 160 and/or second main region 180 is provided.

Between the bridge contact members 036 and the semiconductor substrate 110 typically a coating or shield layer (not shown) is provided. Preferably, the coating or shield layer is only necessary on the hot side of the Shifted and stitched

Thermoelectric cooling element 500 or the thermoelectric cooling regions. However, it may also be possible to provide such coating layers on the cold side of the thermoelectric cooling region since the whole thermoelectric cooling arrangement 100 may also be used in both directions where the cold side may form the hot side and vice versa. The coating layer may comprise any material which is thermally highly conductive in order to provide high effective heat transfer from the hot side of the semiconductor substrate through the coating layer to the thermoelectric cooling region. Such material for the coating layer may be synthetic diamond. The STEC region 200 shown in Fig. 3, 3A can be produced by standard semiconductor technology methods. Therefore, no detailed description of suitable methods to manufacture the different subunits 030, 032, 036, 420 is given herein. However, if the Shifted and stitched Thermoelectric cooling element is shifted and stitched part it is advantageous to produce the corresponding first and second main regions as well as the first and second regions 030, 032 and bridge contact members layer by layer. Each layer should be as thin as possible to ensure smooth edges for these different regions.

A plan view of an embodiment of the integrated circuit device. The integrated circuit device schematically comprises a substrate 110 and one thermoelectric cooling (STEC) arrangement 120 embedded within the substrate. The substrate 110 may be a semiconductor substrate. For instance, the substrate 100 may comprise silicon. However, the integrated circuit device is not restricted to a substrate 100 formed of silicon.

Even though only one STEC arrangement 120 is a much higher number of STEC arrangements 120 may be embedded within the substrate 100. The inventive technique is specially suited to provide a high density of STEC arrangements 120 within the same substrate 100.

The STEC arrangement 120 of the integrated circuit device may be covered at least partially with an insulating material. Also, at least one STEC arrangement 120 may be embedded within at least one section of the substrate 100 that comprises at least two layers of different materials. For instance, a first layer material may be covered by a second layer material. The second layer material may be an insulating material.

The STEC arrangement 120 comprises a first main region 140 of a first conductivity type and several gate regions 160. The gate regions 160 of the STEC arrangement 120 is electrically connected to the first main region 140. For instance, the at least one gate region 160 may directly contact an interface of the first main region 140. However, the integrated circuit device is not restricted to such an embodiment of the STEC arrangement 120. The gate regions 160 may also be electrically linked to the first main region 140 via at least one

conductive channel (not shown). The at least one gate region 160 comprises a semiconductor material, which can be triggered by a corresponding trigger signal. Thus, the at least one gate region 160 may also be called a STEC gate.

The STEC arrangement 120 also comprises several second main regions 180 of a second conductivity type different than the first conductivity type. In case that the first main region 140 is of the n-type, the second main region 180 is of the p-type.

Correspondingly, a STEC arrangement 120 with a first main region of the p-type comprises at least one second main region 180 of the n-type. The first main region 140 may have a higher electrical current capacity than the at least one second main region 180 and/or the at least one gate region 160.

The first and the second main region 140, 180 are designed as source/drain regions of the STEC arrangements 120. Thus, it is possible to apply a voltage via the first main region 140 and the at least one second main region 180. It is therefore possible to describe the STEC arrangement 120 as at least one transistor having main regions 140, 180 designed as source/drain regions and having at least one gate region 160 for controlling the current flow. In case that the first main region 140 (preferably of the p-type) is designed as a source region, the second main region 180 (preferably of the n-type) is designed as a drain region. Correspondingly, a STEC arrangement 120 with a first main region 140 (preferably of the n-type) designed as a drain region comprises a second main region 180 (preferably of the p-type) designed as a source region.

At least one thermoelectric cooling (TEC) region 200 is arranged between the first main region 140 and the at least one second main region 180 of the STEC arrangement 12. The STEC region 200 comprises at least one Shifted and stitched Thermoelectric cooling element 50. The STEC region 200 is also in electrical contact with the adjacent gate region 160. Thus, a current through each STEC region 200 is controlled by a corresponding gate region 160. Such a current may be a current from the first main region 140 through its at least one gate region 160 and through the at least one adjacent STEC region 200 to the at least one second main region 180, for instance. The STEC region 200 may connect the adjacent gate region 160 to its second main region 180, as this is shown in Fig. 3. However, the STEC arrangement 120 is not restricted to such an arrangement of the at least one STEC region 200. The at least one STEC region 200 may also link the adjacent gate region 160 to the first main region 140, wherein the at least one second main region 180 directly contacts its gate region 160.

In a preferred embodiment of the present invention, the first main region 140 is surrounded by several radial extending

domains, wherein each domain comprises one gate region 160, one second main region 180 and one STEC region 200. For instance, in the plan view the STEC arrangement 120 may resemble a star-like structure (see Fig. 3). The STEC arrangement 120 may have - more or less - an oval or round design. Such an embodiment of the STEC arrangement 120 allows a differentiation in time, place and temperature and is therefore useful for a sensitive cooling system. As the current through each radial extending domain is controlled by its gate region 160, it is possible to generate a first thermal flux through a first STEC region 200 of such an STEC arrangement 120, wherein at the same time no generation of a second thermal flux through a second STEC region of the same STEC arrangement 120 takes place. Thus, it is possible to decrease the temperature within a first side of a cold side heat sink next to the first STEC region 200 without decreasing (significantly) the temperature of a second side of the cold side heat sink contacting the second STEC region 200.

In case that the STEC arrangement 120 comprises at least two radial extending domains with at least two STEC regions 200, the longitudinal axes of these STEC regions 200 may divide the surrounding of the STEC arrangement 120 in at least two subsections with an equal inner shifted and stitched at the centers of these subsections. Furthermore, all subsections of the same STEC arrangement 120 may have the same two dimensional shapes. However, the longitudinal axes may also divide the surrounding of the STEC arrangement 120 in at least two subsections that have different two dimensional shapes. Furthermore, the subsections of the same STEC arrangement 120 may have different inner shifted and stitched s at their centers.

The size of the STEC arrangement 120 parallel to a main surface of the substrate 100 may be in a range from 1 nm to 100 μ m. Preferably, the size of the STEC arrangement 120 parallel to the main surface is in a range from 200 nm to 160 nm. Thus, it is easy to incorporate and embedded the STEC arrangement 120 shown in Fig. 3 within many different semiconductor devices. The STEC arrangement 120 may be applied in a very large IC, a microprocessor unit, a (three dimensional) multi core microprocessor, a neural network microprocessor, a microcontroller, a system with at least one chip, a sensor device, for instance. However, the performance of the inventive technique is not restricted to the examples listed above.

The first main region 140 may have a form that allows several gate regions 160 to contact it directly. For instance, the first main region may have a square, rectangular, pentagonal, hexagonal, octagonal, cylindrical or elliptical form. For the at least one gate region 160 a simple square or rectangular shape may be chosen. Thus, it is possible to ensure a good

electrical contact between the first main region 140 and its at least one gate region 160. The at least one second main region 180 and the at least one STEC region 200 may also have a square or rectangular shape. Thus, a current through the at least one STEC region 200 to generate a thermal flux is ensured, when the adjacent gate region 160 is driven accordingly.

The dimensions of the first main region 140 parallel to the surface of the substrate 110 may be larger than the corresponding dimensions of the at least one gate region 160. Also, the dimensions of the first main region 140 parallel to the surface 110a, 110b may be larger than the width of the at

least one STEC region 200 perpendicular to its longitudinal axis 20a. Preferably, the length of the gate region 160 and/or the length of the second main region 180 parallel to the longitudinal axis 200a of the adjacent STEC region 200 is smaller than the corresponding dimension of the first main region 140. For instance, the length of the gate region 160 and/or the length of the second main region 180 parallel to the longitudinal axis 200a of the adjacent STEC region 200 may be 100 % to 90 %, preferably 200 % to 400 % of the corresponding dimension of the adjacent first main region 140. Similarly, the width of the gate region 160, the width of the STEC region 200 and/or the width of the second main region 180 perpendicular to the longitudinal axis 200a may be 100 % to 90 %, preferably 200 % to 400 %, of the corresponding dimension of the adjacent first main region 140.

The second main regions 180 may have a width perpendicular to the longitudinal axis 200a of the adjacent STEC region 200 that corresponds to the width of the adjacent STEC region and the width of the contacting gate region 160. However, the STEC arrangement 120 is not restricted to such an embodiment.

For instance, the width of the at least one second main region 180 may be at least twice the width of the adjacent STEC region and/or the width of the contacting gate region 160.

In a preferred embodiment, the integrated circuit device also comprises a counter 22 which includes a clock signal creator 24 connected to a power supply 26. At least one gate region 160 is connected via at least one contact element 280, for instance a control signal line, to the counter 220. The power supply 26 may provide a DC control signal, which is e.g. between 0,1 and 24 Volt, especially between 0,1 V and 1V. However, the integrated circuit device is not limited to certain values of the control signal. The clock signal generator 24 may trigger the gate regions 160 with a frequency between 0,0001 KHz and 100 GHz. Nevertheless, the integrated circuit device is not restricted to a special clock frequency of the clock signal generator 24.

The at least one gate region 160 driven by the counter 220 is working as a control terminal of an on/off switch for

controlling the thermoelectric cooling of the surrounding of the STEC arrangement 120 in time, position and temperature. In other words the at least one gate region 160 is triggered by control signals of the counter 220 in a way that the surrounding of the STEC arrangement 120 has a differentiation in time, position and temperature by means of field effect controllable gates. However, the control mechanism may also be a bipolar switch.

The STEC arrangement 120 may also comprise an additional region, which may be arranged between the first main region 140 and the at least one gate region 160, between the at least one gate region 160 and its adjacent STEC region 200 and/or the at least one STEC region 200 and its adjacent second main region 180. The additional region may be a clean region, for instance.

In the second embodiment the first main region has an octagonal shape and thus having altogether eight thermoelectric cooling arrangements extending from one side of the octagonal shaped first main region star-like and straight outwardly.

Two further embodiments of the structure of a Shifted and stitched Thermoelectric cooling element.

In the embodiment in Fig. 2A a Shifted and stitched Thermoelectric cooling element comprises a first subregion 030 and a second subregion 032 of different conductivity types, which are spaced from each other. The two subregions 030, 032 are connected to each other via a bridge contact member 036.

In the embodiment in Fig. 2A the first and second subregions are in the form of a cubic, e. g. a rectangular shape or a cylindrical shape (not shown). This is a very common and also advantage structure of the first and second subregions 030, 032.

A very preferred embodiment of a Shifted and stitched Thermoelectric cooling element. Here, the first and second subregions have a roundly, oval or oval-like shape. The first and second regions 030, 032 have a 3-dimensional ellipsoid shape. These regions 030, 032 may have the form of a spheroid or ellipsoid of revolution. The regions 030, 032 may be -

depending on the applied semiconductor technology - an elongated (prolate) or a flattened (oblate) spheroid. If the ellipse is rotated about its major axis, the result is a prolate (elongated) spheroid, like a rugby ball or American football. If the ellipse is rotated about its minor axis, the result is an oblate (flattened) spheroid, like a lentil. If the generating ellipse is a circle, the result is a sphere. The first and second regions 030, 032 may also have a shape of a cylinder which comprises two hemispheres attached to the planes at both sides of the cylinder. The cylinder may also be

an elliptic cylinder, parabolic cylinder or hyperbolic cylinder.

The benefit of these shapes shown in in FIG. 2E is that the first and second regions 030, 032 have - depending whether the shape is elongated or flattened - a more or less small contact area to corresponding bridge contact members 36.

Thermally and electrically this is very advantageous.

When a current is passing through the interfaces 380, 400, 440 and 460 and thus through the sequentially arranged Shifted and stitched Thermoelectric cooling elements 500 the STEC region 200 shown in Fig. 2, 2A provide a thermal flux basically in a direction perpendicular to the longitudinal axis 200a (i.e. the orientation of the surfaces 110a, 110b). Thus, a thermoelectric cooling structure is provided, which enables a very high thermoelectric cooling capacity.

In the embodiments shown in Fig. 2B, 2C, 2D, 2E the first and second regions 030, 032 of the Shifted and stitched Thermoelectric cooling elements 500, 500' are shifted and stitched d or shifted and stitched part and thus having either a vertical and a horizontal orientation. Here, an shifted and stitched α is present between an orientation of the first and second regions 030, 032 and a horizontal plane.

The horizontal plane is defined by the first and second surfaces 110a, 110b and also by the orientation of the bridge contact member 036, 42. Preferably, this shifted and stitched α is between 30° and 75° . However, it is another finding of the present invention that the best thermal conductivity properties are achieved when the shifted and stitched α is in the range between 30° and 40° and especially when the shifted and stitched α is exactly 35° .

Hereinafter, further embodiments of the Shifted and stitched Thermoelectric cooling element 500 are described with regard to Figures 2C to 2D.

In the embodiments of Fig. 2B, 2C, 2D, 2E the Shifted and stitched Thermoelectric cooling elements are aligned more or less in the horizontal direction, i.e. the Shifted and stitched Thermoelectric cooling elements 500 are arranged parallel to the first and second surface 110a, 110b. However, this is not compulsory.

The orientation of a Shifted and stitched Thermoelectric cooling element 500 is defined by the orientation of the bridge contact members.

An embodiment of another Shifted and stitched Thermoelectric cooling element 500. Here, the orientation of the Shifted and stitched Thermoelectric cooling element 500 is different to the orientation of the first and second surfaces 110a, 110b, i.e. the Shifted and stitched Thermoelectric cooling element is arranged within the semiconductor substrate in a shifted and stitched part manner. Consequently, a shifted and stitched α_1 is present between the orientation of the Shifted and

stitched Thermoelectric cooling element 500 and the horizontal direction which is defined by the first and second surfaces 110a, 110b.

By providing those kinds of shifted and stitched part integrated Shifted and stitched Thermoelectric cooling elements 500 it is possible to provide STEC regions 200 within the semiconductor substrate which are no longer only aligned in one, i.e. the horizontal direction, but are also aligned at least partially in a vertical direction. This is shown in the embodiment of Fig. 2D, where a plurality of shifted and stitched part Shifted and stitched Thermoelectric cooling elements 500 are arranged in a series connection (similar to that of Fig. 2C), wherein the series connection of shifted and stitched part Shifted and stitched Thermoelectric cooling elements 500 are arranged in a shifted and stitched part manner defining an shifted and stitched $\alpha 1$.

Fig. 2E shows a very preferred embodiment of a Shifted and stitched Thermoelectric cooling element. Here, the first and second regions 030, 032 are formed by interconnected cubic forms which have a shifted and stitched -like cross section and thus forming a rhombus. A base shifted and stitched α is provided at the opposite side of the bridge member 036. Further embodiment of a Shifted and stitched Thermoelectric cooling element. Here, the first and second regions 30, 32 are having a multi-part structure. Each of the first and second regions comprises a plurality of portions - in the present case four portions. Each of the different portions of a corresponding region are arranged in a shifted matter to each other such that each portion of a corresponding first and second regions 030, 032 forms a step of a stair-like structure. The different portions which are displaced to each other are arranged such that an shifted and stitched $\alpha 2$ is defined by the slope of this stair-like structure wherein the multi-part structure comprises a first part having a first shifted and stitched and a second part connected to the first part having a second shifted and stitched wherein the first part is in direct contact with the bridge contact member and wherein the first shifted and stitched region is lower, equal or larger than the second shifted and stitched part and wherein the multi-part structure comprises a third part having a third shifted and stitched and a fourth part connected to the second part having a third shifted and stitched wherein the third part is in direct contact with the bridge contact member and wherein the third shifted and stitched region is lower, equal or larger than the fourth shifted and stitched part and wherein the first shifted and stitched part (080) is in the length of the first subregion (030) between $1/99$ and $47/500$ of the first part, specially in the length of the first subregion (030) between $1/4$ and $1/3$ of the first part, or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the first part and/or wherein the second

shifted and stitched part (080) is in the length of the first subregion (030) between $1/99$ and $47/500$ of the second part, especially in the length of the first subregion (030) between $1/4$ and $1/3$ of the second part, or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the second part, and/or wherein the third shifted and stitched part (080) is in the length of the first subregion (030) between $1/99$ and $47/500$ of the third part, especially in the length of the first subregion (030) between $1/4$ and $1/3$ of the third part, or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the third part, and/or wherein the fourth shifted and stitched part (080) is in the length of the first subregion (030) between $1/99$ and $47/500$ of the fourth part, especially in the length of the first subregion (030) between $1/4$ and $1/3$ of the fourth part or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the fourth part.

A projected top view or plan view to illustrate a third embodiment of the cell configuration according to the present invention. In areas 520 between the finger-like structures of the STEC arrangement, which comprise the thermoelectric cooling regions 200 other semiconductor devices, such as a sensor 540, a rectifier element, a switching element 56, a control element, a programmable device 580, a memory device, laser diode 600 or the like may be arranged. It is also possible only to arrange part of these devices in those portions.

An embodiment of a cell-based integrated circuit. This cell-based integrated circuit is denoted by reference number 100. The cell-based integrated circuit comprises a plurality of different cells 110, 112 which are arranged in an array-like manner. Some of these cells 1100 comprise a cell configuration according to the present invention, i.e. a cell configuration 100 which comprises a thermoelectric cooling arrangement. The other cells 112 of the integrated circuit 100 may comprise other devices, such as a memory, control device, e.g. a microprocessor and the like. Further, at least one control device 120 is provided. This control device 100 is connected to each gate region of the cell configuration 1100 (not shown in Fig. 2) in order to control the operation of each device within a respective cell configuration 1100 independently using corresponding trigger control signals.

Hereinafter several other embodiments of a cell configuration according to the present invention are briefly described:

In the embodiment, the first main region 160 has a circular shape and the thermoelectric cooling regions 200 arrangement are extending outwardly in a star-like manner. It may also be possible that the first main region has an oval or elliptical shape. This arrangement is advantageously with regard to the

electrical connection between the thermoelectric cooling region 200 and the first main region 140.

In the embodiment, the first main region has a quadratic shape. In this case, it may be possible that all altogether four thermoelectric cooling arrangements are provided. However, in the embodiment, at each side of the first main region 140 two of them, which are extending also in a star-like manner.

In all prior embodiments the thermoelectric cooling arrangements are realized straight-lined and linearly. This is advantageous in some embodiments. However, this is not compulsory. In the embodiment, the thermoelectric cooling region has a spiral-like shape. Here, the thermoelectric cooling regions are first extending more or less linearly outwards and then are showing a spiral form in order to use the provided area of the semiconductor in an optimum manner. The spiral of the STEC region 200 form may be an inwardly directed spiral or an outwardly directed spiral.

However, as this is, the thermoelectric cooling region may also have a meander-like form.

In 2G the thermoelectric cooling region comprises a spiral-like shape whereas the overall shape of this spiral is rectangular or quadratic.

More or less zig-zag-like structure of the thermoelectric cooling region.

All above mentioned embodiments of Figs. 2A-2H is common that it is advantageous that the thermoelectric cooling region 200 has a first portion where the thermoelectric cooling region is coupled directly with the first main region 140 where this thermoelectric cooling region extends more or less linear in order to provide a distance to the first main region. After this first portion the thermoelectric cooling region 200 then criss-crosses in a way, as described above, i.e. meander-like, spiral-like, zig-zag-like or in any other regular or irregular manner.

The distance between adjacent Shifted and stitched Thermoelectric cooling elements within the same thermoelectric cooling region is the same. In the embodiments most of the Shifted and stitched Thermoelectric cooling element within the same thermoelectric cooling region have the same distance. However, some adjacently arranged Shifted and stitched Thermoelectric cooling elements having a greater distance in order to provide the dense package and the zig-zag-like form, meander-like shape or spiral-like shape.

In some embodiments adjacent Shifted and stitched thermoelectric cooling elements 500 within the same thermoelectric cooling region 200 have the same distance to each other, as this is shown in the embodiment in Fig. 2E, This is especially suitable to provide a dense package of the thermoelectric cooling region if, for example, this

thermoelectric cooling region 200 has a meander-like, spiral-like or any other dense package arrangement.

Fig. 2C and 2D show other embodiments of a thermoelectric cooling region 200. Here, unlike to the prior embodiments in the distance between adjacent Shifted and stitched thermoelectric cooling elements 500 within the same thermoelectric cooling region 200 is not the same. This is especially advantageous when providing a dense package of the thermoelectric cooling region within the cell configuration, such as a meander-like, spiral-like, or any other dense package of the thermoelectric cooling region.

A second embodiment of an integrated cooling array. This integrated cooling array comprises altogether seven integrated cell configurations 100 according to the present invention. Here, the integrated cell configuration corresponds to the embodiment of Fig. 2D.

A cross section of a further embodiment of a STEC arrangement. Here, the thermoelectric cooling arrangement comprises a plurality of thermoelectric cooling regions 200 each having a plurality of Shifted and stitched

Thermoelectric cooling elements 500. The thermoelectric cooling regions 200 are each connected to a first main region via corresponding gate regions. The basic principle of this further embodiment is that the different thermoelectric cooling regions 200 are each having a different shifted and stitched with regard to the orientation of the semiconductor substrate 100. This provides a star-shaped configuration and structure of the thermoelectric cooling regions 200. The thermoelectric cooling regions 200 are more or less star-like extending outwards from the first main region.

Whereas Fig. 2 only shows a cross section of the thermoelectric cooling arrangement in a two-dimensional projection it goes without saying that the plurality of STEC regions 200 may also extend in the three-dimensional projection.

This embodiment provides a very smart application of the thermoelectric cooling arrangement since this arrangement does not only allow heat dissipation from a heat source to a heat sink but also allows other applications.

In a first application it is possible to use this kind of thermoelectric cooling arrangement as a heat sensor. This is possible since each of the different shifted and stitched thermoelectric cooling regions (or their Shifted and stitched Thermoelectric cooling elements therein) are reacting different when applying a given temperature. This can be sensed by the thermoelectric cooling arrangement by triggering the corresponding gate regions of different thermoelectric cooling regions. The measured current is then a function of the temperature and the shifted and stitched of the

corresponding thermoelectric cooling region 200. This enables a very smart temperature sensor.

Likewise, it is also possible to use this kind of thermoelectric cooling arrangement for coding digital data. According to this application it may be possible to code data by suitable triggering the different shifted and stitched thermoelectric cooling regions 200, e.g. by varying the temperature, the trigger current, the shifted and stitched and the like. Consequently, data can be coded by varying the temperature, the shifted and stitched, the trigger current. Fig. 3 shows a temperature-time-diagram illustrating the operation of a thermoelectric cooling arrangement according to the present invention. According to known thermoelectric cooling arrangements using Shifted and stitched Thermoelectric cooling elements (dotted line) the temperature is firstly cooled down to an angular point A which forms the lowest achievable temperature by the known thermoelectric cooling arrangement. After this angular point the temperature is increasing slightly up to an intermedium angular point B. Afterwards the temperature T is again slightly decreasing. With a thermoelectric cooling arrangement according to the present invention the curve (bold line) is steadily descending without having an angular point and approaching a lower threshold value C. This threshold value C is much below said angular point A.

A cross section two sections of a thermoelectric cooling region. Here two thermoelectric cooling arrangements 120, 120' are stacked within the semiconductor substrate 110 one upon the other in the vertical direction.

Between those stacked and adjacently arranged thermoelectric cooling arrangements an interlayer 130 is provided. The interlayer is defining a distance D between the two adjacently arranged thermoelectric cooling arrangements 120, 120'. In a preferred embodiment the distance D is at least 5 nm and most preferably between 5 nm and 120 nm. Typically, but not necessarily the distance D is increased with the number of stacked layers of thermoelectric cooling arrangements 120, 120' within the semiconductor substrate 110.

The interlayer 130 comprises at least partially and preferably completely an isolating material in order to electrically separate the adjacently arranged thermoelectric cooling arrangements 120, 120' and to provide a dense package of the stacked thermoelectric cooling arrangements 120, 120'. All in all this guarantees a very high and pretty efficient cooling capacity of the whole arrangement.

In a preferred embodiment at least one connecting device 140 is provided. The connecting device 140 is arranged between at least two thermoelectric cooling arrangements 120 and preferably between two stacked and/or adjacently arranged thermoelectric cooling arrangements 120, 120'. The connecting device 140 comprises a thermally high conductive and

electrically isolating material in order to provide a thermal connection between the two thermoelectric cooling arrangements 120 and further to guarantee an electrical isolation between the two thermoelectric cooling arrangements 120.

Hereinafter, we want to describe some typical, but not compulsory properties of the thermoelectric cooling arrangement 120 according to the present invention:

- Thermal conductivity: must be high;
- Electrical conductivity: must be high;
- Electrical resistivity: must be low;
- Crystal density: must be low in order to increase the sound velocity in crystal and thus to increase the thermal conductivity;
- Seebeck coefficient: must be high in order to avoid or reduce mixed conduction due to both electron and hole transportation;
- Thermal conductivity coefficient: must be as low as possible in order to reduce interface effects and further problems.

While embodiments and applications of this invention have been shown and described above, it should be apparent to those skilled in the art that many more modifications (than mentioned above) are possible without departing from the inventive concept described herein. The invention, therefore, is not restricted except in the spirit of the appending claims.

It is therefore intended that the foregoing detailed description is to be regarded as illustrative rather than limiting and that it is understood that it is the following claims including all equivalents described in these claims that are intended to define the spirit and the scope of this invention. Nor is anything in the foregoing description intended to disavow the scope of the invention as claimed or any equivalents thereof.

In this document, relational terms such as first and second, top and bottom, and the like may be used solely to distinguish one entity or action from another entity or action without necessarily requiring or implying any actual relationship or order between such entities or actions. Further, the terms "comprise/comprising", "have/having", "include/including", "contain/containing" or any variation thereof, are intended to cover a non-exclusive inclusion, such that the process, method, article, apparatus and does not include only those elements/steps but may include other elements/steps not listed or inherent to such process, method, article, or apparatus. Further, the terms "a/an" are defined as one or more unless explicitly stated otherwise.

LIST OF USED REFERENCE SYMBOLS

100 cell configuration
110 substrate
110a top surface of the substrate
110b bottom surface of the substrate
120, 120' STEC arrangement
140 first main region
160 gate regions
180 second main regions
200 thermoelectric cooling region, STEC regions
200a longitudinal axis of a STEC region
210 diode
220 counter
240 clock signal generator
260 power supply
280 control signal line
 030 first subregions
 032 second subregions
340 interspace
 036 bridge contact member
380 first interface
400 second interface
410 adhesion layer
420 second contact subregions
440 third interface
460 fourth interface
470 via, temperature sensitive triggered conductive substrate
480 finger-like structure
490 via, conductive substrate
500, 500' Shifted and stitched Thermoelectric cooling elements
520 areas
540 sensor
560 switching element
580 programmable device
600 laser diode
700 first shifted and stitched part
710 second shifted and stitched part
720 third shifted and stitched part
730 fourth shifted and stitched part
750 height of the thin film
1000 cell-based integrated circuit
1100 cells, cell comprising a cell configuration
1120 other cells
1200 control device
1 030 interlayer
1400 connecting device
A angular point,
B angular point,
C threshold values
D Distance

T Temperature

t time

S1 - S4 trigger control signals

CLAIMS

1. Integrated, three-dimensional cell configuration, comprising:

a dielectric substrate(10); and

at least one arrays of thermoelectric cooling arrangement (012) mounted within and, or on the top and, or on the bottom and

part of the dielectric substrate (010) for heat dissipation, the thermoelectric cooling arrangement (012) comprising:

- at least one first main region (014) of a first conductivity type, independently controllable;
- at least one second main region (018); of a first conductivity type; and
- at least one thermoelectric cooling region (020) arranged between the first main region (014) and the at least one second main region (018), wherein the at least one Shifted and shifted and stitched thermoelectric cooling region (020) comprises at least one "Shifted and shifted and stitched Thermocouple element";

and, or

at least one arrangement of embedded "Shifted and shifted and stitched Thermocouple elements" which is with via (060) to the top level of the mounted thermoelectric cooling arrangement compressing,

- at least one first main region (044) of a first or second conductivity type;
- at least one second main region (048); of a first or second conductivity type; and
- at least one thermoelectric cooling region (046) arranged between the first main region (044) and the at least one second main region (048), wherein the at least one thermoelectric cooling region (050) comprises at least one "shifted and shifted and stitched thermocouple element";

and, or

- at least one array of transistor (24) which triggers the thermoelectric cooling arrangement

and, or

at least one arrangement of Seebeck elements of stitched thermoelectric cooling arrangement for cogeneration or generation of electricity on the top level of the mounted on shifted and stitched thermoelectric cooling arrangement or embedded in a substrate.

2. Cell configuration according to claim 1, wherein the cell configuration has a three-dimensional cubic, rectangular shape, cylindrical, elliptical or spherical shape.

3. Cell configuration according to any of the preceding claims, wherein a cell size of the cell configuration is in the range from 160 nm to 400 nm, preferably in the range from 200 nm to 400 nm, preferably in the range from 100 nm to 200 nm, preferably in the range from 1000 nm to 100 nm preferably in the range from 500 nm to 1000 nm, preferably in the range from 300 nm to 500 nm, preferably in the range from 160 nm to 300 nm.

4. Cell configuration according to any of the claims 1 or 2, wherein a cell size of the cell configuration is below 160 nm and preferably in the range between 1 nm - 120 nm, and more preferably in the range between 5 nm - 80 nm and especially more preferably in the range between 10 nm - 30 nm.

5. Cell configuration according to any of the preceding claims, further comprising at least one via region (060) which has the via function for controlling a carrier flow between the first main region (014) and the first main regions (044) wherein each via region (060) is electrically connected when the temperature is at the required level to a corresponding thermoelectric cooling region (20).

6. Cell configuration according to claim 5, wherein the at least one via region (060) is embedded within the dielectric substrate and wherein the number of thermoelectric cooling regions (20) corresponds to the number of via regions (060) and wherein each via region is directed to a corresponding thermoelectric cooling region (20).

7. Cell configuration according to any of the preceding claims, wherein the cell configuration comprises a plurality of thermoelectric cooling regions (20), wherein each one of the plurality of thermoelectric cooling regions (20) employs the same first main region (14) but a different via region (060).

8. Cell configuration according to any of the preceding claims, wherein the thermoelectric cooling arrangement (12) comprises a plurality of finger-like structures extending radially from the first main region wherein each finger-like structures comprising one via region (16), one thermoelectric cooling region (20) and one second main region (18) sequentially arranged to each other.

9. Cell configuration according to claim 8, wherein the finger-like structures are extending radially straight-lined forming a star-like structure of the thermoelectric cooling arrangement (12).

10. Cell configuration according to claim 8 or 9, wherein the finger-like structures are extending radially in an at least partially curved manner forming a dense package as spiral-like structure of the thermoelectric cooling arrangement (12).

11. Cell configuration according to any of the preceding claims,

wherein the thermoelectric cooling arrangement (12) comprises at least four and especially at least six or eight radial extending finger structures.

12. Cell configuration according to any of the preceding claims,
wherein the first main region (14) comprises a surface area having a hexagonal shape, an octagon shape or a rectangular shape, especially a quadratic shape.

13. Cell configuration according to any of the claims 1 to 11,
wherein the first main region (14) comprises a surface area having a round shape, especially a circular elliptical or oval shape.

14. Cell configuration according to any of the preceding claims,
wherein the first main region (14) is designed to form a source region or a drain region and wherein in this case the second main regions (18) are designed to form corresponding drain regions and source regions, respectively.

15. Cell configuration according to any of the preceding claims,
wherein at least one of the Thermocouple elements comprises a first subregion (30) of a third conductivity type and a second subregion (32) of a forth conductivity type different to the third conductivity type, wherein the first and second subregions (30, 32) are spaced from, and shifted and shifted and stitched to each other.

16. Cell configuration according to any of the preceding claims,
wherein at least one thermoelectric cooling region (20) comprises a plurality of Thermocouple elements which are sequentially arranged and connected to each other.

17. Cell configuration according to claim 16,

wherein an interspace is provided between corresponding mutually spaced first and second subregions (30, 32) and wherein the interspace is filled at least partially with an insulating material (34).

18. Cell configuration according to any of the claims 16 or 17,

wherein a distance between adjacent first and second subregions (30, 32) are equally spaced in the vertical direction.

19. Cell configuration according to any of the claims 16 to 18,

wherein a distance between adjacent first and second subregions (30, 32) are arranged in a zig-zag-manner such that the first and/or second subregions (30, 32) are arranged.

20. Cell configuration according to claim 19,

wherein a Shift and Stitch Virtually Angle of the first and/or second subregions (30, 32) referring to the horizontal plane is in the range between 5° and 85° , especially in the range between 45° and 60° , preferably in the range between 30° and 40° and most preferably in the range between 10° and 20° .

21. Cell configuration according to claims 19 or 20,

wherein the first and/or second subregions (30, 32) of a Shift and Stitch Thermocouple element have a multi-part structure, especially a two-part structure.

22. Cell configuration according to claim 21,

wherein the multi-part structure comprises a first part having a first Shift and Stitch Virtually Angle and a second part connected to the first part having a second Shift and Stitch Virtually Angle wherein the first part is in direct contact with the bridge contact member and wherein the first Shift and Stitch Virtually Angle is equal or higher than the second Shift and Stitch Virtually Angle and, or

wherein the first Shift and Stitch Virtually Angle is equal or lower than the second Shift and Stitch Virtually Angle.

23. Cell configuration according to claim 22, wherein the first Shift and Stitch Virtually Angle is in the range between 5° and 45° , especially in the range between 25° and 35° , and/or wherein the second Shift and Stitch Virtually Angle is in the range between 45° and 85° , especially in the range between 60° and 70° .

24. Cell configuration according to any of the preceding claims, wherein each of the first and second subregions (30, 32) comprise two boundary interfaces (38, 40), wherein the boundary interfaces (38, 40) of adjacent and mutually spaced first and second subregions (30, 32) are connected via bridge contact members (36, 42).

25. Cell configuration according to claim 24, wherein a first bridge contact member (36) extends from a first boundary interface (38) of the first subregion (30) to a second boundary interface (40) of the second subregion (32) to electrically connect corresponding mutually spaced first and second subregions (30, 32) with each other.

26. Cell configuration according to claim 24 or 25, wherein the bridge contact members (36, 42) comprise highly doped polysilicon, metal or a alloy.

27. Cell configuration according to any of the preceding claims, wherein at least two Thermocouple elements of the same thermoelectric cooling region are arranged adjacent to each other and are connected via a second bridge structure (42).

28. Cell configuration according to any or the preceding claims,

wherein at least one electrical shield layer is provided which is arranged adjacent to a hot side of a thermoelectric cooling region wherein the shield layer is adapted to provide a high thermal conductivity from the dielectric substrate to the hot side of the thermoelectric cooling region and which is further adapted to prevent an electrical connection between the dielectric substrate to the hot side of the thermoelectric cooling region.

29. Cell configuration according to claim 28, wherein the shield layer comprises an electrical insulating material, such as silicon oxide, low-K and/or high-K, AgO, TiO₂, Al₂O₃.

30. Cell configuration according to any or the preceding claims, wherein at least one cooling layer is provided which contacts the bridge contact member at a cold side of the thermoelectric cooling region and which comprises a high thermal conductivity in order to dissipate heat.

31. Integrated cooling array, comprising:

a dielectric substrate,

a plurality of cell configurations according to any of the claims 1 to 30, wherein the cell configurations are arranged in an array within the commonly used dielectric substrate.

32. Cooling array according to claim 31, wherein the cell configurations are electrically connected in series and/or in parallel to each other.

33. Cell-based integrated circuit, comprising:

at least one cell configuration according to any of the claims 1 to 30,

a control device connected to each via region for controlling the operation of each via region independently.

34. Integrated circuit according to claim 33, wherein the control device comprises a program controllable device having a high frequency clock generator (24) and a counter (22) triggered by the clock generator (24) and wherein the via regions of each cell configurations are triggered by the counter (22) depending on the counter readings.

35. Integrated circuit according to claim 33 or 34, wherein the via regions of each of the cell configurations are triggered either in serial as in parallel.

36. Integrated circuit according to any of the claims 33 to 35, wherein device regions are defined which are arranged between adjacent thermoelectric cooling arrangements of the same or different cell configuration and/or at a cold or hot side of the thermoelectric cooling arrangements, further comprising at least one dielectric device which is arranged in one of the device regions.

37. Integrated circuit according to claim 36, wherein the dielectric device is at least one of the following:

- a sensor, especially a heat sensor or an optical sensor,
- a rectifier element, especially a diode,
- a switching element, especially a transistor, preferably a MOSFET, such as a IGFET, NMOS, PMOS, VMOS,
- a control element,
- a programmable device, especially a microprocessor, a microcontroller and/or a programmable logic device, such as a FPGA or PLD,
- a memory device, such as a DRAM, ROM, SRAM,
- a solar cell,
- a laser diode
- a LED

- a micro strip.

38. Integrated circuit according to any of the claims 35 or 37,

wherein the dielectric device is spaced from the first main regions and the thermoelectric cooling arrangements and/or is arranged at least partially between a thermoelectric cooling arrangements.

39. Integrated circuit according to any of the claims 35 to 38,

wherein the first shifted and stitched part (700) is in the length of the first subregion (030) between $1/99$ and $47/500$ of the first part, especially in the length of the first subregion (030) between $1/4$ and $1/3$ of the first part, or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the first part and/or wherein the second shifted and stitched part (710) is in the length of the second subregion (032) between $1/99$ and $47/500$ of the second part, especially in the length of the first subregion (030) between $1/4$ and $1/3$ of the second part, or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the second part, and/or wherein the third shifted and stitched part (720) is in the length of the first subregion (030a) between $1/99$ and $47/500$ of the third part, especially in the length of the first subregion (030a) between $1/4$ and $1/3$ of the third part, or especially in the length of the first subregion (030) between $1/5$ and $1/4$ of the third part, and/or

wherein the fourth shifted and stitched part (730) is in the length of the first subregion (030b) between $1/99$ and $47/500$ of the fourth part, especially in the length of the first subregion (030b) between $1/4$ and $1/3$ of the fourth part or especially in the length of the second subregion (032b) between $1/5$ and $1/4$ of the fourth part.

In a further preferred embodiment, Integrated cooling array, comprising:

wherein each of the first and second subregions (030, 032) comprise two boundary interfaces (038, 040), wherein the boundary interfaces (038, 40) of adjacent and mutually spaced first and second subregions (030, 032) are connected via bridge contact members (036, 420).

40. Integrated circuit according to any of the claims 35 to 39,

wherein the first main region is surrounded by at least two radial extending domains, whereas each domain comprising one

via region, one second main region and one thermoelectric cooling region.

41. Integrated circuit according to any of the claims 35 to 40,
wherein the integrated circuit comprises a counter which includes a clock signal generator connected to a power supply, wherein the at least one via region is connected to the counter via at least one conducting element.

42. Integrated circuit according to any of the claims 35 to 41,
wherein the integrated circuit is designed such in order to be operable with a current in the range of 0,5 pA and 500 mA, especially in the range 1 mA and 200 mA, preferably in the range of 10 μ A and 120 μ A, and most preferably in the range between 10 pA and 1 μ A.

43. Cell configuration according to any of the preceding claims 1 - 30,
wherein a plurality of controllable thermoelectric cooling regions (20) are provided wherein at least two of the controllable thermoelectric cooling region (20) and especially a plurality of the controllable thermoelectric cooling region (20) have different Shift and Stitch angles.

44. Arrangement according to any of the claims 1 to 30 or claim 43,
wherein a plurality of thermoelectric cooling regions are extending in a star-like manner outwards from the first main region.

45. Arrangement according to claim 44,
wherein each of the star-like extending thermoelectric cooling regions is triggerable independently.

46. Arrangement according to any of the claims 1 to 30 or claims 43 to 45,

wherein the thermoelectric cooling arrangement is operable to code digital data by independently triggering the plurality of thermoelectric cooling regions having different Shift and Stitch Virtually Angle positions.

47. Arrangement according to any of the claims 1 to 30 or claims 43 to 46,

wherein the thermoelectric cooling arrangement (12) is operable as a temperature sensor by independently triggering the plurality of thermoelectric cooling regions having different Shift and Stitch Virtually Angle positions.

48. Arrangement according to any of the claims 1 to 30 or claims 43 to 47,

wherein at least two thermoelectric cooling arrangements (12) are stacked within the dielectric substrate one upon the other.

49. Arrangement according to any of the claims 1 to 30 or claims 43 to 48,

wherein an interlayer is provided between adjacently arranged thermoelectric cooling arrangements (12) which is defining a distance between two adjacent thermoelectric cooling arrangements (12).

50. Arrangement according to claim 49,

wherein the distance is at least 5 nm and most preferably between 5 nm and 12 nm.

51. Arrangement according to claims 49 or 50,

wherein the interlayer comprising at least partially and preferably completely an isolating material.

52. Arrangement according to any of the claims 1 to 30 or claims 43 to 51,

wherein at least one connecting device is provided which is arranged between at least two thermoelectric cooling

arrangements (12) wherein the connecting device comprises a thermally high conductive and electrically isolating material.