

Description

Title of Invention: DIRECT-POWER-CONVERTER CONTROL DEVICE

Technical Field

[0001] This invention relates to a technique for controlling a direct power converter including a converter, an inverter, and a power buffer circuit that are mutually connected through a DC link.

Background Art

[0002] Generally, full-wave rectifying circuits are used as converters to obtain a DC voltage from a single-phase AC voltage input from a single-phase AC power source. However, the output of the full-wave rectifying circuits contains power ripple having a frequency twice that of the single-phase AC voltage. Thus, reduction in this power ripple requires a power buffer circuit that buffers the power between an output of the full-wave rectifying circuit and a load.

[0003] Non-Patent Documents 1 to 3 and Patent Documents 1 to 4 listed below disclose a technique for connecting a capacitor to a DC link through a switching element. In the proposed technique, the capacitor (hereinafter also referred to as a "buffer capacitor"), which functions as a voltage source, drives a load together with a power supply voltage to compensate for the power ripple as well as reduce the electrostatic capacity required for the buffer capacitor.

[0004] Particularly, Non-Patent Documents 1 to 2 and Patent Documents 1 to 4 also propose a technique that achieves a function of a boost chopper using a reactor and a switch to boost a voltage across a buffer capacitor (hereinafter referred to as a "both-end voltage").

[0005] Non-Patent Document 2 teaches a case (a discontinuous mode) where a reactor current flowing through a reactor is discontinuous to achieve the function of the boost chopper. A command value of the reactor current (hereinafter also referred to as a “reactor current command”) depends on a current to be input to a full-wave rectifying circuit. Non-Patent Document 2 also teaches a technique for estimating the input current by obtaining the maximum value and the minimum value of a both-end voltage.

[0006] Furthermore, Patent Document 2 discloses a technique for maintaining an average of a both-end voltage. Patent Document 3 teaches cases where the reactor current flows not only in the discontinuous mode but also in a critical mode.

10 Prior-Art Documents

Patent Documents

[0007] Patent Document 1: Japanese Patent Application Laid-Open No. 2011-193678

Patent Document 2: Japanese Patent Application Laid-Open No. 2014-107935

Patent Document 3: Japanese Patent No. 5454732

15 Patent Document 4: Japanese Patent Application Laid-Open No. 2014-96976

Non-Patent Documents

[0008]

Non-Patent Document 1: Ohnuma, Itoh, “Circuit Configuration and Control Strategy of single-to-three Phase Power Converter with Active Buffer and Charge Circuit”, The 2010 Annual Meeting of the Institute of Electrical Engineers of Japan, 4-057 (2010)

Non-Patent Document 2: Ohnuma, Itoh, “Experimental Verification of Single Phase to Three Phase Converter Using an Active Buffer circuit with a Charge Circuit”, 2010 IEE-Japan Industry Applications Society Conference, 1-124 (2010)

Non-Patent Document 3: Ohnuma, Itoh, “Basic Investigation and Capacitance Reduction method of A Novel Single-Phase to Three-Phase Power Converter”, The papers of

Technical Meeting on Semiconductor Power Converter, IEE Japan, SPC-08-16 (2008)

Summary of Invention

Problems to be Solved by the Invention

[0009] However, use of film capacitors as the buffer capacitors is undesirable in consideration of downsizing the buffer capacitors. Here, options for capacitors to be used as the buffer capacitors include ceramic capacitors and electrolytic capacitors.

[0010] The tolerance range of the electrostatic capacity of the electrolytic capacitors largely varies from $\pm 20\%$ to $\pm 30\%$. Moreover, the electrostatic capacity tends to decrease according to degradation of the capacitors. When the voltage of the buffer capacitor varies according to change in the electrostatic capacity, an error increases in estimating an input current. This induces variations in the both-end voltage. When the variations are prominent, a direct power converter may not be operable.

[0011] Thus, embodiments of the present invention seek to provide a technique for making variations in the both-end voltage less prominent even when the electrostatic capacity of the buffer capacitor varies.

Means to Solve the Problems

[0012] The direct-power-converter control device according to this invention is a control device (10) that controls a direct power converter.

[0013] The direct power converter includes: a DC link (7) including a first power supply line (LH) and a second power supply line; a converter (3) that receives a single-phase AC voltage (V_{in}), and outputs ripple power (P_{in}) to the DC link in which the first power supply line is higher in potential than the second power supply line; a power buffer circuit (4) provided between the first and second power supply lines, the power buffer circuit buffering power by buffered power (P_{buf}) obtained by multiplying an AC component ($P_{in}^{\wedge}$) of the ripple power (P_{in}) by a distribution factor (k); and an inverter (5)

that converts a DC voltage (V_{dc}) between the first and second power supply lines into an AC voltage.

[0014] The power buffer circuit includes: a discharge circuit (4a) including a capacitor (C4) and a switch (Sc, D42) connected in series with the capacitor between the first and second power supply lines, the switch being closer to the first power supply line relative to the capacitor; and a charge circuit (4b) that charges the capacitor.

[0015] The control device includes an inverter controller (101), a discharge controller (102), and a charge controller (103).

[0016] The inverter controller outputs an inverter control signal (SSup, SSvp, SSwp, SSun, SSvn, SSwn) for controlling an operation of the inverter on the basis of a rectifying duty (drec), a discharge duty (dc), and a command value (V_u^* , V_v^* , V_w^*) of a voltage to be output by the inverter, the rectifying duty being a duty at which the converter is brought into conduction with the DC link, the discharge duty being a duty at which the switch is conducting.

[0017] The discharge controller outputs a discharge switch signal (SSc) for bringing the switch into conduction on the basis of the discharge duty.

[0018] The charge controller includes: an amplitude determining unit (103a) that determines an amplitude (I_m) of an input current (I_{in}) to be input to the converter by performing at least proportional-integral control on a deviation (ΔV_c) between a voltage across the capacitor and an average voltage command value (V_c^*) that is a command value of an average of the voltage across the capacitor; a charge command generating unit (103b) that determines a charge command (i_L^*) on a current (i_l) flowing through the charge circuit by multiplying by the amplitude a function ($F_1(\omega t)$, $F_2(\omega t)$, $F_3(\omega t)$) of a phase (ωt) of the single-phase AC voltage, the function being determined according to the discharge duty, the rectifying duty, and the distribution factor; and a charging operation

controller (103c) that controls a charging operation of the charge circuit on the basis of the charge command.

[0019] For example, the discharge duty and the rectifying duty are set so that the power buffer circuit (4) receives power from the DC link during a period during which a cosine value ($\cos(2\omega t)$) is negative and provides power to the DC link during a period during which the cosine value is positive, the cosine value being a cosine of a value twice the phase (ωt).

[0020] Alternatively, power (P_l) received by the power buffer circuit (4) from the DC link (7) and power (P_c) provided by the power buffer circuit (4) to the DC link (7) are set to vary at a frequency twice a frequency of the single-phase AC voltage (V_{in}) as a fundamental frequency.

[0021] Preferably, the function is determined with the input current (I_{in}) having a sinusoidal waveform.

[0022] Preferably, responsiveness of the charge controller (103) is less than or equal to one tenth of a value twice a frequency of the single-phase AC voltage (V_{in}).

Effects of the Invention

[0023] Even when an electrostatic capacity of a capacitor (buffer capacitor) included in a discharge circuit of a power buffer circuit varies, variations in both-end voltage of the capacitor are made less prominent.

[0024] The objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description and the accompanying drawings.

Brief Description of Drawings

[0025] FIG. 1 is a block diagram illustrating a structure of a direct power converter according to embodiments;

FIG. 2 is a block diagram exemplifying a structure of a control device according to the embodiments;

FIG. 3 is a block diagram schematically illustrating the balance of power in the direct power converter illustrated in FIG. 1;

5 FIG. 4 is a diagram illustrating an equivalent circuit of the direct power converter illustrated in FIG. 1;

FIG. 5 is a graph indicating relationships between an average, the maximum value, the minimum value, and fluctuation of a both-end voltage of a buffer capacitor;

10 FIG. 6 is a graph indicating behaviors of various quantities in a technique corresponding to a technique of Patent Document 2 when an electrostatic capacity of the buffer capacitor decreases;

FIG. 7 is a graph indicating behaviors of various quantities in the technique corresponding to the technique of Patent Document 2 when the electrostatic capacity of the buffer capacitor increases;

15 FIG. 8 is a graph indicating behaviors of various quantities in a first embodiment when the electrostatic capacity of the buffer capacitor decreases;

FIG. 9 is a graph indicating behaviors of various quantities in the first embodiment when the electrostatic capacity of the buffer capacitor increases;

20 FIG. 10 is a graph indicating operations of a direct power converter according to a second embodiment;

FIG. 11 is a graph indicating the operations of the direct power converter according to the second embodiment;

FIG. 12 is a block diagram illustrating an example of a structure for performing control with a DC current;

25 FIGS. 13 and 14 are graphs indicating operations of a direct power converter according

to a third embodiment;

FIG. 15 is a graph indicating behaviors of various quantities in the third embodiment when the electrostatic capacity of the buffer capacitor decreases;

FIG. 16 is a graph indicating behaviors of various quantities in the third
5 embodiment when the electrostatic capacity of the buffer capacitor increases; and

FIG. 17 is a circuit diagram illustrating a modification of the direct power converter illustrated in FIG. 1.

Description of Embodiments

[0026] A. Analysis of problems with conventional techniques

10 Before describing embodiments in detail, problems with the conventional techniques will be analyzed to facilitate understanding of the present invention.

[0027] (i) First conventional technique: In Non-Patent Document 2, the minimum value of the both-end voltage is detected and the maximum value of the both-end voltage is used as a voltage command to control the both-end voltage. However, an average of
15 the both-end voltage is high even when a load of an inverter is low because the maximum value of the both-end voltage is used as the voltage command (see, for example, FIG. 7 of Patent Document 2). The high average induces increase in switching loss of a power buffer circuit.

[0028] (ii) Second conventional technique: Apparently, Patent Document 1 suggests
20 a method for obtaining a reactor current command on the basis of the maximum value and the minimum value of a detected both-end voltage to control an average of the both-end voltage. However, since such a control is significantly influenced by the ripple of a voltage output by a full-wave rectifying circuit, the responsiveness of a control system is

inferior (see, for example, FIG. 10 of Patent Document 2).

[0029] (iii) Third conventional technique: In Patent Document 2, a reactor current command is obtained using an average of a both-end voltage as a voltage command to control the both-end voltage. Accordingly, the average is held constant, thus improving the responsiveness (see, for example, FIG. 6 of Patent Document 2).

[0030] However, in the first to third conventional techniques, an input current is estimated not from the both-end voltage themselves but from an average, the maximum value, and the minimum value of the both-end voltage. Thus, variations in electrostatic capacity of a buffer capacitor increase an error of the input current, which may cause variations in operating point of the both-end voltage.

[0031] This is expressed by an equation. According to the various documents above, it is known that the following Equation (1) holds by introducing an amplitude I_m of an input current I_{in} to be input to a full-wave rectifying circuit, an amplitude V_m and an angular velocity ω of a single-phase AC voltage V_{in} ($= V_m \cdot \sin(\omega t)$, where t denotes a time) to be rectified by the full-wave rectifying circuit, an electrostatic capacity C of a buffer capacitor, and the maximum value V_{cmax} and the minimum value V_{cmin} of a both-end voltage.

[0032]

$$I_m = \frac{\omega \cdot C}{V_m} (V_{cmax}^2 - V_{cmin}^2) \quad (1)$$

[0033] Furthermore, the following Equation (2) holds by introducing an average V_{avg} ($= (V_{cmax} + V_{cmin}) / 2$) of the both-end voltage (see, for example, Patent Document 2).

[0034]

$$I_m = \frac{\omega \cdot C}{V_m} \{2 \cdot V_{avg} \cdot (V_{cmax} - V_{cmin})\} \quad (2)$$

[0035] Furthermore, a reactor current command i_l^* is determined according to the following Equation (3) so that the input current i_{in} has a sinusoidal waveform and a power factor is 1 (that is, $i_{in} = I_m \cdot \sin(\omega t)$). Since the amplitude I_m can be obtained from Equations (1) and (2) as described above, the reactor current command i_l^* depends
 5 on the maximum value V_{cmax} and the minimum value V_{cmin} of the both-end voltage.

[0036]

$$i_l^* = I_m \cdot |\sin(\omega t)| - \frac{I_m}{2 \cdot |\sin(\omega t)|} \quad (3)$$

[0037] When a buffer capacitor is provided, it is known that the following Equation (4) holds by introducing a power P_{out} to be output by an inverter 5 and an both-end voltage
 10 V_c (see, for example, Non-Patent Document 3).

[0038]

$$V_c = \sqrt{V_{avg}^2 - \frac{P_{out}}{\omega \cdot C} \cdot \sin(2\omega t)} \quad (4)$$

[0039] When the maximum value V_{cmax} of the both-end voltage V_c is fixed as a command value as according to the first conventional technique, the average V_{avg} of the
 15 both-end voltage V_c also varies according to variations in the power P_{out} subject to variations in a load. In contrast, when the average V_{avg} is fixed as a command value as according to the third conventional technique, a fluctuation ($V_{cmax} - V_{cmin}$) of the both-end voltage V_c varies.

[0040] For example, FIG. 5 indicates relationships between the average V_{avg} , the
 20 maximum value V_{cmax} , the minimum value V_{cmin} , and the fluctuation ($V_{cmax} - V_{cmin}$) of the both-end voltage V_c when $V_m = 230\sqrt{2}$ (V), $I_m = 16\sqrt{2}$ (A), $P_{out} = 3680$ (W). When the amplitude I_m indicated by Equations (1) and (2) is fixed, an operating point of the both-end voltage V_c is determined by the average V_{avg} , and the maximum

value V_{cmax} , the minimum value V_{cmin} , or the fluctuation ($V_{cmax} - V_{cmin}$) according to these relationships. In other words, it is clear that setting of the operating point of the both-end voltage V_c is flexible.

[0041] In these first to third conventional techniques, when the electrostatic capacity of the buffer capacitor varies, it differs from the electrostatic capacity C to be adopted in Equations (1) and (2). Thus, when the amplitude I_m is estimated by Equations (1) and (2), the reactor current command i_l^* set by (3) is not suitable for the actual electrostatic capacity.

[0042] FIG. 6 is a graph indicating behaviors of various quantities in the third conventional technique (corresponding to the technique of Patent Document 2) when the actual electrostatic capacity of the buffer capacitor after 0.1 second decreases by 30% with respect to the electrostatic capacity before the 0.1 second. Assuming the load of the inverter as a three-phase balanced load, load currents i_u , i_v , and i_w flowing through the load were used.

[0043] As understood from Equation (1), decrease in the actual electrostatic capacity of the buffer capacitor corresponds to an excess of the electrostatic capacity C to be used for calculation when the amplitude I_m is estimated. Thus, the estimated value of the amplitude I_m and the reactor current command i_l^* become excessive, and the average V_{avg} also increases. Furthermore, the excess of the reactor current command i_l^* induces increase in the amplitude I_m of the input current I_{in} .

[0044] Since the average V_{avg} is maintained constant in Equation (2) according to the third conventional technique, the fluctuation ($V_{cmax} - V_{cmin}$) after 0.1 second increases (the difference between the maximum value V_{cmax} and the minimum value V_{cmin} suddenly increases in FIG. 6). Accordingly, increase in the average V_{avg} decreases the reactor current command i_l^* , and then an equilibrium is reached.

[0045] However, the average V_{avg} after reaching the equilibrium is larger, and not only the buffer capacitor but also the switching elements included in the inverter require high breakdown voltages.

[0046] FIG. 7 is a graph indicating behaviors of various quantities in the third conventional technique when the actual electrostatic capacity of the buffer capacitor after 0.1 second increases by 30% with respect to the electrostatic capacity before the 0.1 second.

[0047] Here, the average V_{avg} decreases by operations reverse to those performed in FIG. 6. However, decrease in the average V_{avg} diminishes the function of the boost chopper.

[0048] B. Basic ideas of technique to be proposed

As seen in “A. Analysis of problems with conventional techniques”, when the actual electrostatic capacity of the buffer capacitor varies under control of the both-end voltage V_c with detection of the maximum value V_{cmax} and the minimum value V_{cmin} , the influence on the reactor current command i_l^* increases.

[0049] Although a command value (hereinafter referred to as an “average voltage command value”) V_c^* of an average of the both-end voltage V_c is given in a technique proposed by the present application, the average voltage command value V_c^* is compared not with the average V_{avg} but with the both-end voltage V_c itself. Then, the amplitude I_m is determined at least by performing proportional-integral control on a deviation ΔV_c between the average voltage command value V_c^* and the both-end voltage V_c .

[0050] Then, multiplication of a function (will be described in detail in each of the embodiments to be described later) determined according to the various modes in which a direct power converter is operated, by the amplitude I_m determined on the basis of the deviation ΔV_c yields a charge command (this charge command differs from the reactor

current command i_l^* , which will be described in “C. Structures of power converter and its control device” to be described later) as a basis of the reactor current command i_l^* .

[0051] Accordingly, the reactor current command i_l^* is appropriately determined according to the actual electrostatic capacity of the buffer capacitor, which differs from a case where the reactor current command i_l^* is based on the amplitude I_m estimated from Equations (1) and (2) depending on the electrostatic capacity C .

[0052] C. Structures of power converter and its control device

FIG. 1 is a block diagram illustrating a structure of a direct power converter that can apply in common respective modes to be described in embodiments later. The direct power converter includes a converter 3, a power buffer circuit 4, an inverter 5, and a DC link 7.

[0053] The converter 3 is connected to a single-phase AC power source 1 through, for example, a filter 2. The filter 2 includes a reactor L_2 and a capacitor C_2 . The reactor L_2 is provided between the converter 3 and one of two output terminals of the single-phase AC power source 1. The capacitor C_2 is provided between the two output terminals of the single-phase AC power source 1. The filter 2 removes a high-frequency component of a current. The filter 2 may be omitted. For the sake of simplicity, the function of the filter 2 is disregarded in the following description.

[0054] The DC link 7 includes DC power lines LH and LL.

[0055] For example, a diode bridge is used as the converter 3. The converter 3 includes diodes D_{31} to D_{34} . The diodes D_{31} to D_{34} form a bridge circuit that single-phase full-wave rectifies a single-phase AC voltage V_{in} as an input voltage from the single-phase AC power source 1 to convert the single-phase AC voltage V_{in} to a rectified voltage $V_{rec} (= |V_{in}|)$, and outputs the rectified voltage between the DC power lines LH and LL. A potential higher than a potential applied to the DC power line LL is

applies to the DC power line LH. An input current I_{in} flows from the single-phase AC power source 1 into the converter 3. Then, the converter 3 outputs a current I_{rec} ($= I_{in}$).

[0056] The power buffer circuit 4 includes a discharge circuit 4a and a charge circuit 4b, and provides and receives powers to and from the DC link 7. The discharge circuit 4a includes a capacitor C4 as a buffer capacitor, and the charge circuit 4b boosts the rectified voltage V_{rec} to charge the capacitor C4.

[0057] The discharge circuit 4a further includes a diode D42, and a transistor (here, an insulated gate bipolar transistor: hereinafter abbreviated as an "IGBT") Sc connected in antiparallel to the diode D42. The transistor Sc is connected in series with the capacitor C4 between the DC power lines LH and LL, where the transistor Sc is closer to the DC power line LH relative to the capacitor C4.

[0058] The antiparallel connection mentioned herein means parallel connection in which forward directions are opposite to each other. More specifically, the forward direction of the transistor Sc is a direction from the DC power line LL to the DC power line LH. The forward direction of the diode D42 is a direction from the DC power line LH to the DC power line LL. The transistor Sc and the diode D42 can collectively be understood as one switch element (switch Sc). When the switch Sc is conducting, the capacitor C4 discharges, and provides power to the DC link 7.

[0059] The charge circuit 4b includes, for example, a diode D40, a reactor L4, and a transistor (here, an IGBT) S1. The diode D40 has a cathode and an anode. The cathode is connected between the switch Sc and the capacitor C4. This structure is known as a generally-called boost chopper.

[0060] The reactor L4 is connected between the DC power line LH and the anode of the diode D40. The transistor S1 is connected between the DC power line LL and the

anode of the diode D40. The transistor S1 is connected in antiparallel to a diode D41. The transistor S1 and the diode D41 can collectively be understood as one switch element (switch S1). Specifically, the forward direction of the transistor S1 is a direction from the DC power line LH to the DC power line LL. The forward direction of the diode D41 is
 5 a direction from the DC power line LL to the DC power line LH.

[0061] The capacitor C4 is charged by the charge circuit 4b to generate the both-end voltage V_c higher than the rectified voltage V_{rec} . Specifically, a current is caused to flow from the DC power line LH to the DC power line LL through the switch S1 to accumulate energy in the reactor L4. Then, the switch S1 is turned OFF, so that this
 10 energy is accumulated in the capacitor C4 through the diode D40.

[0062] The both-end voltage V_c is higher than the rectified voltage V_{rec} , so that a current basically does not flow into the diode D42. Thus, whether the switch Sc is conducting or non-conducting depends solely on whether the transistor Sc is conducting or non-conducting. Here, the diode D42 ensures a reverse breakdown voltage when the
 15 both-end voltage V_c is lower than the rectified voltage V_{rec} , and brings a current refluxing from an inductive load 6 to the DC link 7 into reverse conduction when the inverter 5 abnormally stops.

[0063] Furthermore, since the DC power line LH is higher in potential than the DC power line LL, a current basically does not flow into the diode D41. Thus, whether the
 20 switch S1 is conducting or non-conducting depends solely on whether the transistor S1 is conducting or non-conducting. Although the diode D41 is exemplified as a diode for bringing the reverse breakdown voltage or the reverse conduction and as a diode included in the transistor S1 to be materialized by an IGBT, the diode D41 itself does not contribute to any circuit operation.

25 [0064] The inverter 5 converts a DC voltage between the DC power lines LH and LL

into an AC voltage and outputs the AC voltage to output terminals Pu, Pv, and Pw. The inverter 5 includes six switching elements Sup, Svp, Swp, Sun, Svn, and Swn. The switching elements Sup, Svp, and Swp are connected between the output terminals Pu, Pv, and Pw, respectively, and the DC power line LH. The switching elements Sun, Svn, and Swn are connected between the output terminals Pu, Pv, and Pw, respectively, and the DC power line LL. The inverter 5 forms a generally-called voltage source inverter, and includes six diodes Dup, Dvp, Dwp, Dun, Dvn, and Dwn.

[0065] Each of the diodes Dup, Dvp, Dwp, Dun, Dvn, and Dwn is arranged such that its cathode is directed toward the DC power line LH and its anode is directed toward the DC power line LL. The diode Dup is connected in parallel to the switching element Sup between the output terminal Pu and the DC power line LH. Likewise, the diodes Dvp, Dwp, Dun, Dvn, and Dwn are connected in parallel to the switching elements Svp, Swp, Sun, Svn, and Swn, respectively. The output terminals Pu, Pv, and Pw output the load currents i_u , i_v , and i_w , respectively, which form a three-phase AC current. For example, IGBTs are used as the switching elements Sup, Svp, Swp, Sun, Svn, and Swn.

[0066] The inductive load 6 is, for example, a rotary machine, and is illustrated by an equivalent circuit representing an inductive load. Specifically, a reactor L_u and a resistor R_u are connected in series. One end of this series connection is connected to the output terminal Pu. This applies to a reactor L_v and a resistor R_v and to a reactor L_w and a resistor R_w . The opposite ends of these series connections are connected to each other.

[0067] When a control system is exemplified using the inductive load 6 as a synchronous machine, a velocity sensor 9 senses the load currents i_u , i_v , and i_w that flow through the inductive load 6 and provides a control device 10 for the direct power converter with a rotational angular velocity ω_m , a q-axis current I_q , and a d-axis current

I_d that are obtained on the basis of the load currents i_u , i_v , and i_w .

[0068] The control device 10 receives an amplitude V_m of the single-phase AC voltage V_{in} , an angular velocity ω (or a phase $\theta = \omega t$ that is a product of the angular velocity ω and a time t), a command value ω_m^* of the rotational angular velocity, a command value V_q^* of a q-axis voltage, a command value V_d^* of a d-axis voltage, the both-end voltage V_c , and a voltage V_l , besides the rotational angular velocity ω_m , the q-axis current I_q , and the d-axis current I_d . Here, the voltage V_l is a voltage to be applied to the reactor L_4 .

[0069] FIG. 2 is a block diagram exemplifying a structure of the control device 10.

10 The control device 10 includes an inverter controller 101, a discharge controller 102, and a charge controller 103.

[0070] The inverter controller 101 outputs inverter control signals SS_{up} , SS_{vp} , SS_{wp} , SS_{un} , SS_{vn} , and SS_{wn} , on the basis of a discharge duty d_c and a rectifying duty d_{rec} , which will be described later in "D. Outline of operations of power buffer circuit 4", and

15 command values V_u^* , V_v^* , and V_w^* output by the inverter 5. The inverter control signals SS_{up} , SS_{vp} , SS_{wp} , SS_{un} , SS_{vn} , and SS_{wn} control operations of the switching elements Sup , Svp , Swp , Sun , Svn , and Swn , respectively.

[0071] The inverter controller 101 includes an output voltage command generating unit 1011 that generates the command values V_u^* , V_v^* , and V_w^* on the basis of the phase $\theta = \omega t$, the q-axis current I_q , the d-axis current I_d , and the rotational angular velocity ω_m and its command value ω_m^* .

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[0072] The inverter controller 101 further includes an amplitude modulation command unit 1012, a sum-of-products arithmetic unit 1013, a comparator 1014, and an arithmetic logic unit 1015.

25 [0073] The amplitude modulation command unit 1012 controls an operation of the

sum-of-products arithmetic unit 1013 on the basis of the discharge duty d_c and the rectifying duty d_{rec} . The sum-of-products arithmetic unit 1013 (illustrated only by multiplication signs for the sake of simplicity) calculates sums of products of the command values V_u^* , V_v^* , and V_w^* , the discharge duty d_c , and the rectifying duty d_{rec} to generate signal waves M . The comparator 1014 outputs results of comparison in value between the signal waves M and a carrier CA to the arithmetic logic unit 1015. The arithmetic logic unit 1015 performs logical operations on the results to output the inverter control signals SS_{up} , SS_{vp} , SS_{wp} , SS_{un} , SS_{vn} , and SS_{wn} .

[0074] The discharge controller 102 includes a duty arithmetic unit 1021 and a comparator 1022. The duty arithmetic unit 1021 receives, according to the various modes in which the direct power converter is operated, a DC voltage V_{dc} or a DC current I_{dc} that can be used by the inverter 5 through the DC link 7 besides the phase θ , the amplitude V_m , and the both-end voltage V_c , and generates the discharge duty d_c and the rectifying duty d_{rec} . Since the methods for generating the discharge duty d_c and the rectifying duty d_{rec} differ according to the various modes in which the direct power converter is operated, the methods will be described in the respective embodiments to be described later.

[0075] The comparator 1022 compares the discharge duty d_c with the carrier CA to generate a discharge signal SS_c for bringing the switch Sc into conduction.

[0076] Since such operations by the inverter controller 101 and the comparator 1022 are based on known techniques (for example, Non-Patent Documents 1 and 2 and Patent Document 1), the detailed operations are omitted herein.

[0077] However, in the following embodiments, the output voltage command generating unit 1011 sometimes requires the amplitudes V_m , the amplitude I_m (determined on the basis of the deviation ΔV_c as above), and a distribution factor k ($0 \leq k$

≤ 1) to be described later in "D. Outline of operations of power buffer circuit 4" to generate the command values V_u^* , V_v^* , and V_w^* .

[0078] The charge controller 103 includes an amplitude determining unit 103a, a charge command generating unit 103b, and a charging operation controller 103c.

5 [0079] The amplitude determining unit 103a includes a subtractor 1031 and a proportional integral controller 1032. The subtractor 1031 obtains the deviation ΔV_c from the both-end voltage V_c and an average voltage command value V_c^* . The proportional integral controller 1032 performs proportional-integral control on the deviation ΔV_c to determine the amplitude I_m . The amplitude I_m influences the
10 command values V_u^* , V_v^* , and V_w^* which influence the operations of the inverter 5 that reduces the deviation ΔV_c . Thus, at least the proportional-integral control on the deviation ΔV_c suffices for determining the amplitude I_m . Obviously, an element that performs proportional-integral-differential control may be used instead of the proportional integral controller 1032.

15 [0080] The charge command generating unit 103b includes a charge waveform table 1033 and a multiplier 1034. The charge waveform table 1033 receives the distribution factor k and the phase $\theta = \omega t$, and outputs a function $F(\theta)$ ($= F(\omega t)$) on the phase θ . The multiplier 1034 multiplies the amplitude I_m by the function $F(\omega t)$ to determine a charge command i_L^* . Since the function $F(\omega t)$ differs for each of the embodiments, it will be
20 described individually in each of the embodiments.

[0081] The charging operation controller 103c controls an operation of the charge circuit 4b on the basis of the charge command i_L^* . More specifically, the charging operation controller 103c generates a charge switch signal SSl for controlling the switch Sl so that the reactor current i_l flowing through the reactor $L4$ is equal to the reactor
25 current command i_l^* corresponding to the charge command i_L^* . Since the voltage V_l is

necessary to generate this charge switch signal SS1, it is input to the charging operation controller 103c.

[0082] The charging operation controller 103c functions as, for example, a critical mode modulator that generates the charge switch signal SS1 so that the reactor current i_l flows in the critical mode. In Non-Patent Document 2, the value of the inductance of the reactor L4 is limited on the premise that the reactor current i_l flows in the discontinuous mode. However, according to the technique proposed by the present application, even when the inductance varies from the limits and influences the both-end voltage V_c , the operation of the amplitude determining unit 103a accommodates the influence of variations.

[0083] With such structures, the technique described in “B. Basic ideas of technique to be proposed” can be embodied.

[0084] D. Outline of operations of power buffer circuit 4

Instantaneous input power P_{in} to be input to the converter 3 is expressed by the following Equation (5) with an input power factor 1.

[0085]

$$\begin{aligned} P_{in} &= V_m \cdot I_m \cdot \sin^2(\omega t) \\ &= \frac{V_m \cdot I_m}{2} - \frac{V_m \cdot I_m}{2} \cdot \cos(2\omega t) \end{aligned} \quad (5)$$

[0086] The instantaneous input power P_{in} has an AC component ($-\frac{1}{2} \cdot V_m \cdot I_m \cdot \cos(2\omega t)$ (hereinafter may be referred to as an “AC component $P_{in}^{\wedge}$ ”))

indicated by the second term in the right side of Equation (5). Thus, the instantaneous input power P_{in} may be hereinafter referred to as ripple power P_{in} .

[0087] The power converter illustrated in FIG. 1 can be understood as follows.

[0088] The converter 3 receives the single-phase AC voltage V_{in} , and outputs the ripple power P_{in} . The power buffer circuit 4 receives receiving power P_1 from the DC

link 7, and outputs providing power P_c to the DC link 7. The inverter 5 receives input power $P_{dc} (= P_{in} + P_c - P_l)$ obtained by subtracting the receiving power P_l from a sum of the ripple power P_{in} and the providing power P_c , and outputs the load currents i_u , i_v , and i_w . If the loss of the inverter 5 is disregarded, the input power P_{dc} is equal to the power

5 P_{out} (see Equation (4)).

[0089] FIG. 3 is a block diagram schematically illustrating the balance of power in the direct power converter illustrated in FIG. 1. The power subjected to buffering (hereinafter referred to as "buffering power P_{buf} ") is equal to a power difference ($P_c - P_l$) obtained by subtracting the receiving power P_l from the providing power P_c .

10 Furthermore, power P_{rec} transferred from the converter 3 to the inverter 5 is equal to $(P_{in} - P_l)$. Thus, $P_{dc} = P_{rec} + P_c$ holds.

[0090] A distribution factor k is introduced into the next Equation (6).

[0091]

$$P_{dc} = \frac{V_m \cdot I_m}{2} - (1 - k) \cdot \frac{V_m \cdot I_m}{2} \cdot \cos(2\omega t) \quad (6)$$

15 [0092] In other words, when $k = 0$, the inverter 5 receives the ripple power P_{in} as it is in as the input power P_{dc} from the DC link 7. This means $P_{buf} = 0$ which corresponds to a case where no power is distributed to the power buffer circuit 4. When $k=1$, $P_{dc} = P_{in} - P_{in}^{\wedge}$ holds. This corresponds to a case where the power buffer circuit 4 provides and receives to and from the DC link 7 powers of the absolute value $|P_{in}^{\wedge}|$ of the AC component $P_{in}^{\wedge}$.

20

[0093] In other words, the distribution factor k indicates a level of the absolute value $|P_{in}^{\wedge}|$ of the AC component $P_{in}^{\wedge}$ to be distributed to the power buffer circuit 4 as the buffering power P_{buf} .

[0094] E. Equivalent circuit of direct power converter and various duties

FIG. 4 illustrates an equivalent circuit of the direct power converter illustrated in FIG. 1. The equivalent circuit is introduced by, for example, Non-Patent Document 2 and Patent Documents 1, 3, and 4. In the equivalent circuit, a current i_{rec1} is shown equivalently as the current i_{rec1} flowing through a switch S_{rec} when the switch S_{rec} is conducting. Likewise, a discharge current i_c is shown equivalently as the discharge current i_c flowing through the switch S_c when the switch S_c is conducting.

[0095] Furthermore, a current flowing into the inductive load 6 through the inverter 5 when the output terminals P_u , P_v , and P_w are commonly connected to one of the DC power lines LH and LL in the inverter 5 is also shown equivalently as a zero current i_z flowing through a switch S_z when the switch S_z is conducting.

[0096] Furthermore, FIG. 4 shows the reactor L_4 , the diode D_{40} , and the switch S_I that are included in the charge circuit 4b, and the current i_l flowing through the reactor L_4 .

[0097] Then, duties d_{rec} , d_c , and d_z in which the switches S_{rec} , S_c , and S_z are brought into conduction, respectively, are introduced in the equivalent circuit thereby formed.

As known by the documents above, $0 \leq d_{rec} \leq 1$, $0 \leq d_c \leq 1$, $0 \leq d_z \leq 1$, and $d_{rec} + d_c + d_z = 1$ hold.

[0098] Since the duty d_{rec} is a duty for setting a period during which the converter 3 is connected to the DC link 7 to allow a current to flow through the inverter 5, it is the rectifying duty d_{rec} .

[0099] Since the duty d_c is a duty at which the capacitor C_4 discharges, it is the discharge duty d_c .

[0100] Since the duty d_z is a duty at which the zero current i_z always flows irrespective of an output voltage in the inverter 5, it may be called a zero duty d_z .

[0101] Since the currents i_{rec1} , i_c , and i_z are obtained by multiplying the duties d_{rec} , d_c , and d_z , respectively, by the DC current I_{dc} to be input to the inverter 5, the currents

i_{rec1} , i_c , and i_z are averages in switching periods of the switches S_{rec} , S_c , and S_z , respectively. Thus, the duties d_{rec} , d_c , and d_z can be regarded as current distribution factors of the DC current I_{dc} relative to the currents i_{rec1} , i_c , and i_z , respectively.

[0102] When a diode bridge is used as the converter 3, the converter 3 cannot actively perform a switching operation in the rectifying duty d_{rec} . Thus, the inverter 5 and the switch S_c perform a switching operation at the zero duty d_z and the discharge duty d_c , respectively, thus obtaining the current i_{rec1} .

[0103] During a period in which the zero current i_z flows, the inverter 5 cannot use a DC voltage in the DC link 7. Thus, the DC voltage in the DC link 7 to be used in supplying power to the inverter 5 is significant in converting power. In other words, the instantaneous DC voltage that is not used by the inverter 5 for power conversion is meaningless even in considering a voltage utilization factor. The DC voltage V_{dc} significant in converting power can be expressed by Equation (7) below.

[0104]

$$V_{dc} = V_{rec} \cdot d_{rec} + V_c \cdot d_c + 0 \cdot d_z \quad (7)$$

[0105] In contrast, the DC voltage V_{dc} can be understood as a voltage to be applied to the DC link 7 as an average of the maximum values of the voltage that the inverter 5 can output in a period during which switching of the switches S_c and S_l and the inverter 5 is controlled. This is because the inverter 5 is insulated from one of the DC power lines LL and LH during a period corresponding to the zero duty d_z , though the inverter 5 may contribute to the voltage at the DC link 7 at a ratio indicated by the zero duty d_z .

[0106] In FIG. 4, the DC voltage V_{dc} is shown as a voltage across a current source I_{dc} (that supplies the DC current I_{dc}) representing the inverter 5 and a load of the inverter 5.

[0107] Hereinafter, the various modes in which the direct power converter is operated will be specifically described.

[0108] F. First embodiment

The first embodiment will be described in comparison with the operations of the direct power converter introduced by Patent Document 2.

[0109] In the technique disclosed by Patent Document 2, different controls have been alternately performed per quarter period (1/4 period) of the single-phase AC voltage V_{in} (hereinafter, such a control will be also referred to as "quarter period control" for convenience) to cancel out the AC component $\hat{P}_{in}$. Specifically, a control where $P_l = \hat{P}_{in}$ and $P_c = 0$ and a control where $P_l = 0$ and $P_c = -\hat{P}_{in}$ have been alternately performed per quarter period of the single-phase AC voltage V_{in} . Accordingly, $P_{dc} = P_{in} + P_c - P_l = P_{in} - \hat{P}_{in} = (1/2) \cdot V_m \cdot I_m$ holds during all the periods, and the power ripple has been avoided. This holds when $k = 1$ in Equation (6).

[0110] In the present application, a period during which the receiving power P_l is received from the DC link 7 (a period during which a cosine value $\cos(2\omega t)$ that is a cosine of a value twice a phase ωt is negative) is called a receiving period, and a period during which the providing power P_c is provided to the DC link 7 (a period during which the cosine value $\cos(2\omega t)$ is positive) is called a providing period, similarly as Patent Document 2.

[0111] (f-1) Setting of duty

In Patent Document 2, the discharge duty d_c is set by the next Equation (8), and the reactor current command i_l^* is determined by Equation (3) using this discharge duty d_c and on the premise that the input current I_{in} has a sinusoidal waveform. Here, the DC current I_{dc} can be set as a command value.

[0112]

$$d_c = \begin{cases} 0(\text{receivingperiod}) \\ \frac{V_m \cdot I_m}{2 \cdot V_c \cdot I_{dc}} \cdot \cos(2\omega t)(\text{providingperiod}) \end{cases} \quad (8)$$

[0113] Furthermore, the rectifying duty d_{rec} is set by the next Equation (9), thus allowing the DC voltage V_{dc} to have a constant value (for example, Patent Document 1).

[0114]

$$d_{rec} = \begin{cases} \frac{I_m}{2 \cdot I_{dc} \cdot |\sin(\omega t)|} (\text{receivingperiod}) \\ \frac{I_m}{I_{dc}} \cdot |\sin(\omega t)| (\text{providingperiod}) \end{cases} \quad (9)$$

5 [0115] In the first embodiment, the duty arithmetic unit 1021 generates the duties d_c and d_{rec} according to Equations (8) and (9), respectively, using the amplitude I_m obtained from the amplitude determining unit 103a as the amplitude I_m in Equations (3), (8), and (9). In other words, the duty arithmetic unit 1021 receives the amplitudes V_m and I_m , the DC current I_{dc} , and the phase ωt in the first embodiment.

10 [0116] However, the input power P_{dc} to be input to the inverter 5 from the DC link 7 is equal to a product of the DC voltage V_{dc} and the DC current I_{dc} . Since the inverter 5 receives the input power P_{dc} ($= P_{in} + P_c - P_l$) obtained by subtracting the receiving power P_l from a sum of the ripple power P_{in} and the providing power P_c , Equation (10) below holds.

15 [0117]

$$I_{dc} = \frac{P_{in} + P_c - P_l}{V_{dc}} = \frac{V_m \cdot I_m}{2 \cdot V_{dc}} \quad (10)$$

[0118] Thus, Equations (8) and (9) may be modified into Equations (11) and (12), respectively. The DC voltage V_{dc} may be input to the duty arithmetic unit 1021 as a command value, instead of the DC current I_{dc} .

20 [0119]

$$d_c = \begin{cases} 0 (\text{receivingperiod}) \\ \frac{V_{dc}}{V_c} \cdot \cos(2\omega t) (\text{providingperiod}) \end{cases} \quad (11)$$

[0120]

$$d_{rec} = \begin{cases} \frac{V_{dc}}{V_m} \cdot \frac{1}{|\sin(\omega t)|} & (\text{receiving period}) \\ \frac{2 \cdot V_{dc}}{V_m} \cdot |\sin(\omega t)| & (\text{providing period}) \end{cases} \quad (12)$$

[0121] (f-2) Reactor current i_L

In the critical mode, the reactor current i_L rises from 0 to a peak value during a period ΔT_1 during which the switch S1 is conducting, and drops from the peak value to 0 during a period ΔT_2 during which the switch S1 is non-conducting. Such periods ΔT_1 and ΔT_2 are alternately set. When these rise and drop approximate linear change in the time, the reactor current i_L that is half the peak value flows in average.

[0122] Considering that the rectified voltage $V_{rec} = |V_{in}| = V_m \cdot |\sin(\omega t)|$ is applied to the power buffer circuit 4, the period ΔT_1 is expressed by Equation (13) below to which an inductance L of the reactor L4 is introduced.

[0123]

$$\Delta T_1 = \frac{2 \cdot i_L \cdot L}{V_m \cdot |\sin(\omega t)|} \quad (13)$$

[0124] Thus, the period ΔT_1 during which the switch S1 is conducting is determined by Equation (14) using the reactor current command i_L^* expressed by Equation (3) as the reactor current i_L in Equation (13).

[0125]

$$\Delta T_1 = \frac{2 \cdot L}{V_m} \cdot I_m \cdot \left(1 - \frac{1}{2 \cdot \sin^2(\omega t)} \right) \quad (14)$$

[0126] In Equation (14), the amplitude I_m can be obtained from the amplitude determining unit 103a, and the coefficient $2 \cdot L / V_m$ can be regarded as a proportional gain for a voltage control system. Thus, once the charge command i_L^* to be expressed by

Equations (15) is determined, the period $\Delta T1$ is determined by voltage feedback control.

[0127]

$$iL^* = Im \cdot F1(\omega t)$$

$$F1(\omega t) = 1 - \frac{1}{2 \cdot \sin^2(\omega t)} \quad (15)$$

5 [0128] Here, the function $F1(\omega t)$ is the same as the function $F(\omega t)$ above, and is a function of the phase $\theta (= \omega t)$ to be used in the first embodiment. As described in “B. Basic ideas of technique to be proposed”, the charge command iL^* is determined by a product of the amplitude Im and the function $F1(\omega t)$.

[0129] Then, the function $F1(\omega t)$ is determined according to the discharge duty dc 10 determined by Equation (8) or (11), the rectifying duty $drec$ determined by Equation (9) or (12), and the distribution factor k that is equal to 1.

[0130] The charging operation controller 103c operates a counter until reaching the charge command iL^* , and converts the counted value into the period $\Delta T1$ of the charge switch signal $SS1$ (during which the switch $S1$ is conducting). The conversion factor of 15 the counter also functions as a proportional gain for a voltage control system, similarly as the coefficient $2 \cdot L/Vm$.

[0131] When the period $\Delta T1$ starts to be counted for the charge switch signal $SS1$ is the timing when the switch $S1$ is turned ON, which is triggered by the voltage Vl decreasing to 0 that is to be applied to the reactor $L4$. This is because the switch $S1$ may be 20 switched from OFF to ON in the critical mode when the reactor current il decreases to 0 and because the timing with which the reactor current il decreases to 0 can be regarded as the timing with which the voltage Vl decreases to 0.

[0132] (f-3) Advantages

FIGS. 8 and 9 are graphs each indicating behaviors of various quantities when

the technique proposed by the first embodiment is adopted. FIG. 8 indicates a case where the actual electrostatic capacity of the buffer capacitor after 0.1 second decreases by 30% with respect to the electrostatic capacity before the 0.1 second, and FIG. 9 indicates a case where the actual electrostatic capacity of the buffer capacitor after 0.1 second increases by 30% with respect to the electrostatic capacity before the 0.1 second.

[0133] As understood from the comparison between FIGS. 8 and 6 and the comparison between FIGS. 9 and 7, although variations in the fluctuation V_c ($V_{cmax} - V_{cmin}$) remain, variations in the amplitude I_m and in the peak value of the reactor current command i_l^* according to the technique proposed by the first embodiment are smaller than those when the technique of Patent Document 2 has been adopted. The average of the amplitudes I_m is approximately 23 A.

[0134] In order to reduce variations in the amplitude I_m , the responsiveness of the charge controller 103 is preferably less than or equal to one tenth of a value twice the frequency ($\omega/(2\pi)$) of the single-phase AC voltage V_{in} . More specifically, the control bandwidth of the amplitude determining unit 103a, particularly, of the proportional integral controller 1032 is preferably less than or equal to one tenth of the fundamental frequency of the rectified voltage V_{rec} . This is because variations in the amplitude I_m decrease at 20 dB/dec according to decrease in the control bandwidth.

[0135] As described above according to the first embodiment, even when the actual electrostatic capacity of the buffer capacitor varies, variations in the peak value of the reactor current command i_l^* are suppressed and thus prominent variations in the both-end voltage V_c are avoided.

[0136] G. Second embodiment

The second embodiment will describe a case where the distribution factor k , the

rectifying duty d_{rec} , and the discharge duty d_c are different in value from those used in the first embodiment.

[0137] The discharge duty d_c and the rectifying duty d_{rec} expressed by Equations (11) and (12) allow the DC voltage V_{dc} to be constant. This can be understood from the fact that Equation (7) identically holds in consideration of $V_{rec} = V_m \cdot |\sin(\omega t)|$.

[0138] However, during $d_{rec} \leq 1$ and a providing period, $|\sin(\omega t)| \leq 1/\sqrt{2}$ holds. Thus, as seen from the rectifying duty during the providing period in the right side of Equation (12), as long as the DC voltage V_{dc} is maintained constant, the value never exceed $1/\sqrt{2}$ of the amplitude V_m .

[0139] The second embodiment introduces a technique for improving a ratio R of the DC voltage V_{dc} to the amplitude V_m (hereinafter referred to as a “voltage utilization factor”) by adopting the next Equation (16) expressing the DC voltage V_{dc} , thus indicating a function $F_2(\omega t)$ that is a function $F(\omega t)$ when the technique is adopted.

[0140]

$$V_{dc} = \begin{cases} V_m \cdot |\sin(\omega t)| (\text{receivingperiod}) \\ V_m \cdot |\cos(\omega t)| (\text{providingperiod}) \end{cases} \quad (16)$$

[0141] The following description will describe, in order, the probability that the voltage utilization factor R may exceed $1/\sqrt{2}$ by setting the DC voltage V_{dc} through Equation (16), existence of the rectifying duty d_{rec} and the discharge duty d_c for (though approximately) obtaining the DC voltage V_{dc} , and the reactor current command i_l^* and the function $F_2(\omega t)$ when the DC voltage V_{dc} is set.

[0142] (g-1) Improvement in voltage utilization factor R

An average R_a of the voltage utilization factors R during a receiving period is obtained from the next Equation (17). Furthermore, since each phase difference between the providing period and the receiving period and between a sinusoidal

waveform and a cosine waveform is $\pi/2$, the average R_a during the providing period is equal to that during the receiving period.

[0143]

$$\begin{aligned} R_a &= \frac{1}{V_m} \cdot \frac{1}{\pi/2} \cdot \int_{\pi/4}^{3\pi/4} V_m \cdot |\sin(\omega t)| d(\omega t) \\ &= \frac{2\sqrt{2}}{\pi} = \frac{4}{\pi} \cdot \frac{1}{\sqrt{2}} \end{aligned} \quad (17)$$

- 5 [0144] Thus, during any of the providing period and the receiving period, the voltage utilization factors R have been improved in average to $4/\pi$ (>1) times that indicated in the first embodiment.

[0145] (g-2) Setting of duty

- 10 According to the second embodiment, $d_{rec} = 1$ and $d_c = 0$ hold during the receiving period. Such rectifying duty d_{rec} and discharge duty d_c satisfy and can set respective conditions applied thereto, that is, $0 \leq d_{rec} \leq 1$, $0 \leq d_c \leq 1$, and $d_{rec} + d_c + d_z = 1$.

[0146] Accordingly, a result of the calculation of the right side of Equation (7) is equal to the right side for the receiving period in Equation (16).

- 15 [0147] During the providing period, the rectifying duty d_{rec} and the discharge duty d_c are set by Equation (18) and Equation (19), respectively.

[0148]

$$d_{rec} = \sqrt{2} \cdot |\sin(\omega t)| (\text{providingperiod}) \quad (18)$$

[0149]

20
$$d_c = \frac{V_m}{V_c} \cdot \cos(2\omega t) (\text{providingperiod}) \quad (19)$$

[0150] Since $0 \leq |\sin(\omega t)| \leq 1/\sqrt{2}$ holds during the providing period, the rectifying duty d_{rec} set by Equation (18) satisfies the condition $0 \leq d_{rec} \leq 1$ applied thereto.

Furthermore, since $0 \leq \cos(2\omega t) \leq 1$ holds during the providing period, the discharge duty d_c set by Equation (19) satisfies $0 \leq d_c \leq 1$, and $d_{rec} + d_c + d_z = 1$ by increasing the both-end voltage V_c more than the amplitude V_m . For the following convenience, a voltage ratio $\alpha = V_c/V_m$ is introduced herein.

- 5 [0151] The DC voltage V_{dc} during the providing period can be obtained from the next Equation (20) by setting the rectifying duty d_{rec} and the discharge duty d_c as described above.

[0152]

$$\begin{aligned} & V_{rec} \cdot d_{rec} + V_c \cdot d_c + 0 \cdot d_z \\ &= V_m \cdot \sqrt{2} \cdot \sin^2(\omega t) + V_m \cdot \cos(2\omega t) \quad (20) \\ &= \frac{V_m}{\sqrt{2}} \left[1 + (\sqrt{2} - 1) \cdot \cos(2\omega t) \right] \end{aligned}$$

- 10 [0153] Equation (20) approximates Equation (16) well when, for example, the phase ωt takes a value ranging from $3\pi/4$ to $5\pi/4$ during the providing period. Specifically, it is known that a difference in integral value over the providing period between the DC voltage V_{dc} expressed by Equation (16) and the DC voltage V_{dc} expressed by Equation (20) is less than 1%.

- 15 [0154] As described above, satisfying $d_c = d_z = 0$ during the receiving period and using the duty d_{rec} and the duty d_c expressed by Equation (18) and Equation (19) allow the waveforms of the DC voltage V_{dc} to be approximated to the ones expressed by Equation (16), thus improving the voltage utilization factors R .

[0155] (g-3) Reactor current i_l

- 20 During the providing period, the discharge duty d_c expressed by Equation (19) adopted in the second embodiment is V_m/V_{dc} times that in Equation (11) adopted in the first embodiment. Since $V_{dc}/V_m = 2\sqrt{2}/\pi$ holds in the second embodiment as clarified from Equation (17), the discharge duty d_c according to the second embodiment is $\pi/(2\sqrt{2})$

times that according to the first embodiment.

[0156] Thus, the amount of charge to be provided to the DC link 7 by the discharge current i_c during the providing period according to the second embodiment is $k \cdot \pi/(2\sqrt{2})$ times that according to the first embodiment in consideration of the distribution factor k .

5 Thus, the reactor current i_l flowing during the receiving period has to be $k \cdot \pi/(2\sqrt{2})$ times that according to the first embodiment. Thus, the reactor current command i_l^* is set by the next Equation (21) in consideration of Equation (3).

[0157]

$$i_l^* = \text{Im} \cdot \left(|\sin(\omega t)| - \frac{1}{2 \cdot |\sin(\omega t)|} \right) \cdot k \cdot \frac{\pi}{2\sqrt{2}} \quad (21)$$

10 [0158] Thus, Equations (22) yield the function $F2(\omega t)$ in the second embodiment from Equations (15) and (21).

[0159]

$$\begin{aligned} i_L^* &= \text{Im} \cdot F2(\omega t) \\ F2(\omega t) &= F1(\omega t) \cdot \frac{k \cdot \pi}{2\sqrt{2}} \\ &= \frac{k \cdot \pi}{2\sqrt{2}} \left[1 - \frac{1}{2 \cdot \sin^2(\omega t)} \right] \end{aligned} \quad (22)$$

15 [0160] The function $F2(\omega t)$ is determined according to the distribution factor k , the discharge duty d_c which is determined at value 0 during the receiving period and determined by Equation (19) during the providing period, and the rectifying duty d_{rec} which is determined at value 1 during the receiving period and determined by Equation (18) during the providing period.

20 [0161] As seen from the current i_{rec} indicated by FIGS. 10 and 11 to be described later, a sinusoidal waveform of the input current i_{in} as the basis of Equation (3) does not hold

in the second embodiment. Thus, strictly speaking, application of Equation (3) is not rational to obtain Equations (22).

[0162] However, in consideration of the overall receiving period, Equation (3) holds even when the input current I_{in} does not have a sinusoidal waveform. Thus, the function

5 $F2(\omega t)$ may be determined with the input current I_{in} having a sinusoidal waveform also according to the second embodiment.

[0163] In other words, considering that the reactor current i_l flows only during the receiving period, a product of the rectified voltage V_{rec} and the reactor current command i_l^* expressed by Equation (3) suffices the AC component $\hat{P}_{in}$.

10 [0164] Calculating the product yields the next Equation (23), thus clarifying that the product $V_{rec} \cdot i_l^*$ is equal to the AC component $\hat{P}_{in}$.

[0165]

$$\begin{aligned} V_{rec} \cdot i_l^* &= V_m \cdot |\sin(\omega t)| \cdot I_m \cdot \left(|\sin(\omega t)| - \frac{1}{2 \cdot \sin(\omega t)} \right) \\ &= V_m \cdot I_m \cdot \left[\sin^2(\omega t) - \frac{1}{2} \right] \\ &= -\frac{V_m \cdot I_m}{2} \cdot \cos(2\omega t) \end{aligned} \quad (23)$$

[0166] Since Equations (6) and (10) hold independent of the rectifying duty d_{rec} and
15 the discharge duty d_c , the DC current I_{dc} is obtained from the next Equation (24) using Equations (6) and (10) also in the second embodiment. Here, the DC voltage V_{dc} is approximated by Equation (16).

[0167]

$$I_{dc} = \frac{P_{dc}}{V_{dc}} = \frac{V_m \cdot I_m}{2 \cdot V_{dc}} [1 - (1-k) \cdot \cos(2\omega t)] \quad (24)$$

20 [0168] Accordingly, the charge command i_L^* can be obtained using the function $F2(\omega t)$ according to the second embodiment similarly as the function $F1(\omega t)$ according to

the first embodiment. Furthermore, the prominent variations in the both-end voltage V_c are avoided even when the actual electrostatic capacity of the buffer capacitor varies similarly as in the first embodiment.

[0169] (g-4) Behaviors of various quantities

5 FIGS. 10 and 11 are graphs each representing operations of the direct power converter illustrated in FIG. 1 when the duties d_{rec} , d_c , and d_z are set according to the second embodiment. FIG. 10 illustrates a case where $k = 1$, whereas FIG. 11 illustrates a case where $k = 1/3$.

[0170] In both FIGS. 10 and 11, the topmost tier illustrates the duties d_{rec} , d_c , and d_z ,
10 the tier second from the top illustrates the DC voltage V_{dc} (see Equation (16)), the voltages $V_{rec} \cdot d_{rec}$ and $V_c \cdot d_c$ (see Equation (7)) that are included in the DC voltage V_{dc} , and the DC current I_{dc} (see Equation (24)), the tier third from the top illustrates the currents i_{rec} , i_c , i_l , and i_{rec1} , and the bottom tier illustrates the instantaneous powers P_{in} , P_{out} , and P_{buf} . Furthermore, the symbols T_1 and T_2 denote the providing period and
15 the receiving period, respectively.

[0171] In both FIGS. 10 and 11, the horizontal axis represents the phase ωt using “degree” as the unit. Furthermore, the currents I_{dc} , i_{rec} , i_c , i_l , and i_{rec1} have been converted using the amplitude I_m as $\sqrt{2}$. The voltages $V_{rec} \cdot d_{rec}$ and $V_c \cdot d_c$ have been converted using the amplitude V_m as 1, and $\alpha = 1.5$ was set. The instantaneous powers
20 P_{in} , P_{out} , and P_{buf} are obtained as respective products of the voltages and the currents that have been converted as above. Since the reactor current i_l is zero during the providing period T_1 , the current i_{rec1} matches the current i_{rec} . With $d_c = 0$ during the receiving period T_2 , the voltage $V_{rec} \cdot d_{rec}$ matches the DC voltage V_{dc} .

[0172] Since the duties d_{rec} and d_c do not depend on the distribution factor k as
25 described above, the DC voltage V_{dc} and the voltages $V_{rec} \cdot d_{rec}$ and $V_c \cdot d_c$ that are

included in the DC voltage V_{dc} have the same waveforms in both FIGS. 10 and 11.

[0173] However, since the DC current I_{dc} is expressed by Equation (24) and depends on the distribution factor k , it largely differs between $k = 1$ in FIG. 10 and $k = 1/3$ in FIG. 11.

5 [0174] The currents i_c and i_l in the tier third from the top in FIG. 11 where $k = 1/3$ are reduced more than those in FIG. 10 where $k = 1$. Such reduction in the currents i_l and i_c is preferable in view of reduction in the power capacitance required for the reactor L_4 and the capacitor C_4 that are used in the power buffer circuit 4, and downsizing the reactor L_4 and the capacitor C_4 and reduction in their costs.

10 [0175] (g-5) Example of technique for distributing ripple of power according to distribution factor k

This section will describe an example of a technique for satisfying Equation (24) and distributing the ripple of power according to the distribution factor k .

[0176] In this example, operations on a normal AC load are dq-axis controlled which is well known. The power equation on the dq-axis is generally expressed by Equation (25). The symbols V^* and I denote a command value of a voltage to be applied to the AC load and a current flowing through the AC load, respectively. Since these are alternating, a dot representing a complex number is on each of the symbols V^* and I . Note that a q-axis voltage and a d-axis voltage ideally follow a command value (hereinafter referred to as a "q-axis voltage command value") V_q^* and a command value (hereinafter referred to as a "d-axis voltage command value") V_d^* , respectively.

15
20

[0177]

$$P + jQ = \dot{V}^* \cdot \dot{I} = V_d^* \cdot I_d + V_q^* \cdot I_q + j(V_q^* \cdot I_d - V_d^* \cdot I_q) \quad (25)$$

[0178] Since the power supplied from the DC power lines LH and LL to the inverter 5 has no reactive power, the power is expressed by Equation (26) with disregard of the

25

second term of Equation (25).

[0179]

$$P_{dc} = V_d^* \cdot I_d + V_q^* \cdot I_q \quad (26)$$

[0180] Thus, control can be performed by matching the AC component of Equation

5 (26) with the second term in the right side of Equation (6) to satisfy Equation (24). FIG.

12 is a block diagram illustrating an example of a structure for performing the control.

The structure is provided for, for example, the output voltage command generating unit 1011 in FIG. 2.

[0181] First, portions based on the prior art in the structure of FIG. 12 will be simply

10 described. Trigonometric function values $\cos\beta^*$ and $-\sin\beta^*$ are obtained from a current phase command value β^* , and a q-axis current command value I_q^* and a d-axis current command value I_d^* are generated from the obtained trigonometric function values $\cos\beta^*$ and $-\sin\beta^*$ and a current command value I_a^* . Assuming the inductive load 6 as a rotary

15 machine, a q-axis voltage command value V_q^* and a d-axis voltage command value V_d^* are obtained on the basis of the rotational angular velocity ω_m , a field flux Φ_a , a d-axis inductance L_d , and a q-axis inductance L_q of the rotary machine, the q-axis current command value I_q^* , the d-axis current command value I_d^* , a q-axis current I_q , and a d-axis current I_d . Then, voltage command values V_u^* , V_v^* , and V_w^* are generated to control the inverter 5 using the q-axis voltage command value V_q^* and the d-axis voltage
20 command value V_d^* .

[0182] In the structure illustrated in FIG. 1, for example, the velocity sensor 9 senses the load currents i_u , i_v , and i_w flowing through the inductive load 6, and provides the control device 10 with the rotational angular velocity ω_m , the q-axis current I_q , and the d-axis current I_d based on the load currents i_u , i_v , and i_w .

25 [0183] Hereinafter, a processor 71 that performs the control for matching the AC

component of Equation (26) with the second term in the right side of Equation (6) will be described. The processor 71 includes a DC power calculator 711, a ripple component extractor 712, a ripple component calculator 713, a subtractor 714, an adder 715, and a PI processor 716.

5 [0184] The DC power calculator 711 receives the q-axis voltage command value V_q^* , the d-axis voltage command value V_d^* , the q-axis current I_q , and the d-axis current I_d , and calculates the input power P_{dc} on the basis of Equation (26) and provides it to the ripple component extractor 712.

[0185] The ripple component extractor 712 extracts and outputs the AC component of
10 Equation (6). The ripple component extractor 712 is, for example, a high-pass filter (HPF).

[0186] The ripple component calculator 713 receives the amplitudes V_m and I_m , the angular velocity ω , and the distribution factor k , and obtains the second term in the right side of Equation (6). The ripple component calculator 713 can receive the amplitude
15 V_m and the angular velocity ω as information obtained from the single-phase AC power source 1 (see FIG. 1). The ripple component calculator 713 can receive the amplitude I_m from the amplitude determining unit 103a.

[0187] As described above, the desired process is to match the AC component of Equation (26) with the second term in the right side of Equation (6). Thus, the control
20 may be performed by reducing a difference between the output of the ripple component extractor 712 and the output of the ripple component calculator 713. Accordingly, the subtractor 714 calculates the difference. The PI processor 716 performs proportional-integral control on the difference, and outputs a resulting value to the adder 715.

25 [0188] The adder 715 corrects the current command value I_a^* in normal processes,

using the output of the PI processor 716. Specifically, a subtractor 701 calculates a deviation between the rotational angular velocity ω_m and its command value ω_m^* as the normal processes for obtaining the current command value I_a^* . A PI processor 702 performs proportional-integral control on the deviation to temporarily obtain the current command value I_a^* . Then, the adder 715 increases the current command value I_a^* using the output from the PI processor 716.

[0189] Then, the q-axis voltage command value V_q^* and the d-axis voltage command value V_d^* are generated by applying the known technique to the current command value I_a^* corrected by the processor 71 in such a manner. Such a control is performed by applying feedback to the q-axis voltage command value V_q^* , the d-axis voltage command value V_d^* , the q-axis current I_q , and the d-axis current I_d so that the difference output from the subtractor 714 converges to 0. In other words, such a control enables the AC component of Equation (26) to be matched with the second term in the right side of Equation (6).

[0190] H. Third embodiment

(h-1) Setting of duty

The third embodiment does not adopt the quarter-period control adopted in the first and second embodiments. In other words, the rectifying duty d_{rec} and the discharge duty d_c are defined without particularly distinguishing between the receiving period and the providing period in the third embodiment. However, the rectifying duty d_{rec} and the discharge duty d_c do not depend on the distribution factor k , similarly as the first and the second embodiments.

[0191] Specifically, the rectifying duty d_{rec} and the discharge duty d_c are determined by Equation (27) and Equation (28), respectively.

[0192]

$$d_{rec} = \frac{V_{dc}}{V_m} \cdot |\sin(\omega t)| \quad (27)$$

[0193]

$$\begin{aligned} d_c &= \frac{V_{dc}}{V_c} \cdot \cos^2(\omega t) \\ &= \frac{V_{dc}}{2 \cdot V_c} \cdot [1 + \cos(2\omega t)] \end{aligned} \quad (28)$$

[0194] Although the both-end voltage V_c contains ripples to be described later, it is maintained almost constant. Thus, the discharge duty d_c is in direct proportion to $[1 + \cos(2\omega t)]$, and varies at a frequency twice that of the single-phase AC voltage V_{in} as a fundamental frequency. Since the discharge duty d_c is defined without distinguishing between the receiving period and the providing period in the third embodiment as described above, the providing power P_c provided by the power buffer circuit 4 to the DC link 7 also varies at the frequency twice that of the single-phase AC voltage V_{in} as a fundamental frequency.

[0195] Equation (29) is obtained from Equations (27) and (28). Accordingly, Equation (7) identically holds. Thus, the DC voltage V_{dc} can be set to a constant value.

[0196]

$$\begin{aligned} &V_{rec} \cdot d_{rec} + V_c \cdot d_c + 0 \cdot d_z \\ 15 \quad &= V_m \cdot |\sin(\omega t)| \cdot \frac{V_{dc}}{V_m} \cdot |\sin(\omega t)| + V_{dc} \cdot \cos^2(\omega t) \quad (29) \\ &= V_{dc} \end{aligned}$$

[0197] Furthermore, $0 \leq d_{rec} \leq 1$ is satisfied under $V_{dc} \leq V_m$. Furthermore, setting the DC voltage V_{dc} lower than or equal to the both-end voltage V_c can establish a setting that satisfies $0 \leq d_c \leq 1$ and $d_{rec} + d_c + d_z = 1$.

[0198] (h-2) Reactor current i_l

20 Next, the reactor current i_l required to satisfy Equation (6), that is, the reactor

current command i_l^* is obtained. Since the input power P_{dc} is expressed by a product of the DC voltage V_{dc} and the DC current I_{dc} as described above, the current i_{rec1} is obtained by the next Equation (30) from Equations (24) and (27).

[0199]

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$$\begin{aligned} i_{rec1} &= d_{rec} \cdot I_{dc} \\ &= \frac{V_{dc}}{V_m} \cdot |\sin(\omega t)| \cdot \frac{V_m \cdot I_m}{2 \cdot V_{dc}} \cdot [1 - (1 - k) \cdot \cos(2\omega t)] \\ &= \frac{I_m}{2} \cdot |\sin(\omega t)| \cdot [1 - (1 - k) \cdot \cos(2\omega t)] \end{aligned} \quad (30)$$

[0200] Then, the reactor current command i_l^* is determined by the next Equation (31) so that the input current i_{in} has a sinusoidal waveform. As understood from Equation (31), the reactor current command i_l^* varies at the frequency twice that of the single-phase AC voltage V_{in} as a fundamental frequency. Furthermore, the rectified voltage V_{rec} varies in the same manner. Thus, the receiving power P_l received by the power buffer circuit 4 from the DC link 7 also varies at the frequency twice that of the single-phase AC voltage V_{in} as a fundamental frequency.

[0201] Consequently, both the receiving power P_l and the providing power P_c are set to vary at the frequency twice that of the single-phase AC voltage V_{in} as a fundamental frequency according to the third embodiment.

[0202]

$$\begin{aligned} i_l^* &= I_m \cdot |\sin(\omega t)| - i_{rec1} \\ &= \frac{I_m}{2} \cdot |\sin(\omega t)| \cdot [1 + (1 - k) \cdot \cos(2\omega t)] \end{aligned} \quad (31)$$

[0203] Furthermore, Equations (32) can yield a function $F_3(\omega t)$ from Equation (31) according to the third embodiment.

[0204]

$$i_L^* = I_m \cdot F_3(\omega t)$$

$$F_3(\omega t) = \frac{1 + (1-k) \cdot \cos(2\omega t)}{2} \quad (32)$$

[0205] The function $F_3(\omega t)$ is determined according to the discharge duty d_c determined by Equation (28), the rectifying duty d_{rec} determined by Equation (27), and the distribution factor k .

5 [0206] (h-3) Behaviors of various quantities

FIGS. 13 and 14 are graphs each representing operations of the direct power converter illustrated in FIG. 1 when the duties d_{rec} , d_c , and d_z are set according to the third embodiment. FIG. 13 illustrates a case where $k = 1$, whereas FIG. 14 illustrates a case where $k = 1/3$.

10 [0207] In both FIGS. 13 and 14, the topmost graph illustrates the duties d_{rec} , d_c , and d_z , the graph second from the top illustrates the DC voltage V_{dc} (see Equation (29)), the voltages $V_{rec} \cdot d_{rec}$ and $V_c \cdot d_c$ (see Equation (7)) that are included in the DC voltage V_{dc} , and the DC current I_{dc} (see Equation (24)), the graph third from the top illustrates the currents i_{rec} , i_c , i_L , and i_{rec1} , and the bottom graph illustrates the instantaneous powers

15 P_{in} , P_{out} , and P_{buf} .

[0208] In both FIGS. 13 and 14, the horizontal axis represents the phase ωt using “degree” as the unit. Furthermore, the currents I_{dc} , i_{rec} , i_c , i_L , and i_{rec1} have been converted using the amplitude I_m as $\sqrt{2}$, and $R = 0.96$ and $\alpha = 1.5$ were set. The voltages $V_{rec} \cdot d_{rec}$ and $V_c \cdot d_c$ have been converted using the amplitude V_m as 1. The

20 instantaneous powers P_{in} , P_{out} , and P_{buf} are obtained as respective products of the voltages and the currents that have been converted as above.

[0209] Since the duties d_{rec} and d_c do not depend on the distribution factor k as described above, the DC voltage V_{dc} and the voltages $V_{rec} \cdot d_{rec}$ and $V_c \cdot d_c$ that are included in the DC voltage V_{dc} have the same waveforms in both FIGS. 13 and 14.

[0210] However, since the DC current I_{dc} is expressed by Equation (24) and depends on the distribution factor k , it largely differs between $k = 1$ in FIG. 13 and $k = 1/3$ in FIG. 14. Particularly, when $k = 1$, the DC current I_{dc} becomes constant with the constant DC voltage V_{dc} , independent of the phase ωt .

5 [0211] It is clear that the third embodiment can adopt the structure introduced in “(g-5) Example of technique for distributing ripple of power according to distribution factor k ”.

[0212] The currents i_c and i_l in the graph third from the top in FIG. 14 where $k = 1/3$ are reduced more than those in FIG. 13 where $k = 1$. Such reduction in the currents i_l and i_c is preferable in view of reduction in the power capacitance required for the reactor
10 L4 and the capacitor C4 that are used in the power buffer circuit 4, and downsizing the reactor L4 and the capacitor C4 and reduction in their costs.

[0213] (h-4) Advantages

FIGS. 15 and 16 are graphs each indicating behaviors of various quantities when the technique proposed by the third embodiment is adopted. FIG. 15 indicates a
15 case where the actual electrostatic capacity of the buffer capacitor after 0.1 second decreases by 30% with respect to the electrostatic capacity before the 0.1 second, and FIG. 16 indicates a case where the actual electrostatic capacity of the buffer capacitor after 0.1 second increases by 30% with respect to the electrostatic capacity before the 0.1 second.

[0214] Although the input power P_{dc} is the same in the first and third embodiments,
20 the amplitudes of the load currents i_u , i_v , and i_w in the third embodiment are smaller than those in the first embodiment because the voltage utilization factor R in the third embodiment is 0.96 whereas the voltage utilization factor R in the first embodiment is $1/\sqrt{2}$ (≈ 0.71).

[0215] As understood from the comparison between FIGS. 15 and 6 and the
25 comparison between FIGS. 16 and 7, although variations in the fluctuation (V_{cmax} –

V_{emin}) remain, variations in the amplitude I_m and in the peak value of the reactor current command i_L^* according to the technique proposed by the third embodiment are smaller than those when the technique of Patent Document 2 has been adopted. The average of the amplitudes I_m is approximately 23 A as according to the first embodiment.

5 [0216] In order to reduce variations in the amplitude I_m , the responsiveness of the charge controller 103 is preferably less than or equal to one tenth of a value twice the frequency ($\omega/(2\pi)$) of the single-phase AC voltage V_{in} as described in the first embodiment.

[0217] Accordingly, the charge command i_L^* can be obtained using the function $F3(\omega t)$ according to the third embodiment similarly as the function $F1(\omega t)$ according to the first embodiment. Furthermore, the prominent variations in the both-end voltage V_c are avoided even when the actual electrostatic capacity of the buffer capacitor varies similarly as in the first embodiment.

[0218] I. Modifications

15 The filter 2 can be provided between the converter 3 and the power buffer circuit 4 in any of the techniques described above.

[0219] FIG. 17 is a circuit diagram illustrating only the vicinity of the filter 2 provided between the converter 3 and the power buffer circuit 4 as the modification.

[0220] When such a structure is adopted, a diode D_o is preferably provided in the DC power line LH and between the filter 2 and the discharge circuit 4a. The anode of the diode D_o is disposed closer to the filter 2, and the cathode thereof is disposed closer to the discharge circuit 4a.

[0221] The diode D_o can prevent the voltage V_c across the capacitor $C4$ from
25 influencing the both-end voltage of the capacitor $C2$ through switching of the switch S_c .

This advantage is introduced by, for example, Patent Document 4.

[0222] While the invention has been shown and described in detail, the foregoing description is in all aspects illustrative and does not restrict the invention. It is therefore understood that numerous modifications and variations can be devised without departing

5 from the scope of the invention.

CLAIMS

1. A direct-power-converter control device that controls a direct power converter,

said direct power converter including:

a DC link including a first power supply line and a second power supply line;

5 a converter that receives a single-phase AC voltage, and outputs ripple power to said DC link in which said first power supply line is higher in potential than said second power supply line;

a power buffer circuit provided between said first and second power supply lines, said power buffer circuit buffering power by buffered power obtained by multiplying an AC component of said ripple power by a distribution factor; and

10 an inverter that converts a DC voltage between said first and second power supply lines into an AC voltage,

said power buffer circuit including:

a discharge circuit including a capacitor and a switch connected in series with said capacitor between said first and second power supply lines, said switch being closer to said first power supply line relative to said capacitor; and

a charge circuit that charges said capacitor,

said control device comprising an inverter controller, a discharge controller, and a charge controller,

20 wherein said inverter controller outputs an inverter control signal for controlling an operation of said inverter on the basis of a rectifying duty, a discharge duty, and a command value of a voltage to be output by said inverter, said rectifying duty being a duty at which said

converter is brought into conduction with said DC link, said discharge duty being a duty at which said switch is conducting,

said discharge controller outputs a discharge switch signal for bringing said switch into conduction on the basis of said discharge duty, and

5 said charge controller includes:

an amplitude determining unit that determines an amplitude of an input current to be input to said converter by performing at least proportional-integral control on a deviation between a voltage across said capacitor and an average voltage command value that is a command value of an average of said voltage across said capacitor;

10 a charge command generating unit that determines a charge command on a current flowing through said charge circuit by multiplying by said amplitude a function of a phase of said single-phase AC voltage, said function being determined according to said discharge duty, said rectifying duty, and said distribution factor; and

15 a charging operation controller that controls a charging operation of said charge circuit on the basis of said charge command.

2. The direct-power-converter control device according to claim 1,

20 wherein said discharge duty and said rectifying duty are set so that said power buffer circuit receives power from said DC link during a period during which a cosine value is negative and provides power to said DC link during a period during which said cosine value is positive, said cosine value being a cosine of a value twice said phase.

3. The direct-power-converter control device according to claim 1,

wherein power received by said power buffer circuit from said DC link and power provided by said power buffer circuit to said DC link are set to vary at a frequency twice a frequency of said single-phase AC voltage as a fundamental frequency.

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4. The direct-power-converter control device according to one of claims 1 to 3,

wherein said function is determined with said input current having a sinusoidal waveform.

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5. The direct-power-converter control device according to claim 1,

wherein responsiveness of said charge controller is less than or equal to one tenth of a value twice a frequency of said single-phase AC voltage.

6. The direct-power-converter control device according to claim 2,

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wherein responsiveness of said charge controller is less than or equal to one tenth of a value twice a frequency of said single-phase AC voltage.

7. The direct-power-converter control device according to claim 3,

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wherein responsiveness of said charge controller is less than or equal to one tenth of a value twice a frequency of said single-phase AC voltage.

8. The direct-power-converter control device according to claim 4,

wherein responsiveness of said charge controller is less than or equal to one tenth of a value twice a frequency of said single-phase AC voltage.

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