

## CLAIMS

1. A synchronization circuit, comprising M group synchronization signal generating circuits and a node synchronization signal generating circuit, M being a positive integer, wherein

an input terminal of each group synchronization signal generating circuit in the M group synchronization signal generating circuits is for connecting to N nodes, N being a positive integer, and N being greater than or equal to M;

an output terminal of each group synchronization signal generating circuit in the M group synchronization signal generating circuits is connected to the node synchronization signal generating circuit;

an output terminal of the node synchronization signal generating circuit is for connecting to the N nodes;

the group synchronization signal generating circuit is for generating a synchronization indication signal; and

the node synchronization signal generating circuit is for generating a synchronization signal based on the synchronization indication signal generated by the group synchronization signal generating circuit;

wherein each group synchronization signal generating circuit in the M group synchronization signal generating circuits comprises a node synchronization indicating module, a synchronization ready signal generating module, and a group node synchronization indication signal generating module, wherein

the node synchronization indicating module is for indicating to-be-synchronized nodes in the N nodes;

the synchronization ready signal generating module is for generating a synchronization ready signal when each node in the to-be-synchronized nodes is ready for synchronization; and

the group node synchronization indication signal generating module is for generating the synchronization indication signal based on the synchronization ready signal.

2. The synchronization circuit according to claim 1, wherein the synchronization ready signal generating module comprises a shielding module and a synchronization determining module;

the shielding module is for receiving synchronization ready indication signals from the N nodes, and generating an output signal according to indication of the node synchronization indicating module; and

the synchronization determining module is for determining, according to the output signal of the shielding module, whether each node in the to-be-synchronized nodes is ready for synchronization, and generating the synchronization ready signal when it is determined that each node in the to-be-synchronized nodes is ready for synchronization.

3. The synchronization circuit according to claim 2, wherein the shielding module comprises N output signal generating modules, the N output signal generating modules are in one-to-one correspondence with the N nodes, and the shielding module is further for:

generating, for the to-be-synchronized nodes indicated by the node synchronization indicating module, in response to receiving the synchronization ready indication signals from the to-be-synchronized nodes, a first output signal through the output signal generating modules corresponding to the to-be-synchronized nodes; and

generating, for nodes other than the to-be-synchronized nodes indicated by the node synchronization indicating module in the N nodes, a second output signal through the output signal generating modules corresponding to the nodes other than the to-be-synchronized nodes in the N nodes.

4. The synchronization circuit according to any one of claims 1 to 3, wherein the group node synchronization indication signal generating module is further for:

generating, in response to receiving the synchronization ready signal, the synchronization indication signal corresponding to the to-be-synchronized nodes indicated by the node synchronization indicating module.

5. The synchronization circuit according to claim 4, wherein the node synchronization signal generating circuit comprises N output terminals, the N output terminals are respectively for connecting to the N nodes, and the node synchronization signal generating circuit is further for:

generating the synchronization signal corresponding to the to-be-synchronized nodes indicated by the node synchronization indicating module in response to receiving the synchronization indication signal corresponding to the to-be-synchronized nodes; and

sending the synchronization signal through output terminals corresponding to the to-be-synchronized nodes in the N output terminals.

6. The synchronization circuit according to claim 4, wherein the node synchronization indicating module comprises a register, the register comprises at least N register bits, the N register bits are in one-to-one correspondence with the N nodes, register bits that correspond to the to-be-synchronized nodes in the N register bits are configured as a first value, and register bits that correspond to nodes other than the to-be-synchronized nodes in the N nodes in the N register bits are configured as a second value.

7. The synchronization circuit according to claim 6, wherein values of the at least N register bits are configured according to a configuration instruction received by the group synchronization signal generating circuit.

8. A synchronization chip, comprising the synchronization circuit according to any one of claims 1 to 7 and N nodes, wherein the synchronization chip further comprises:

N first synchronization dedicated communication lines, wherein the N first synchronization dedicated communication lines are in one-to-one correspondence with the N nodes, and the N first synchronization dedicated communication lines are respectively for transmitting synchronization ready indication signals from the N nodes to the synchronization circuit.

9. The synchronization chip according to claim 8, wherein the synchronization chip further comprises:

N second synchronization dedicated communication lines, wherein the N second synchronization dedicated communication lines are in one-to-one correspondence with the N nodes, and the N second synchronization dedicated communication lines are respectively for transmitting the synchronization signal from the synchronization circuit to the N nodes.

10. The synchronization chip according to claim 9, wherein the synchronization chip further comprises a processing unit, and the processing unit is for:

determining a first node from the N nodes; and

selecting one group synchronization signal generating circuit from the M group synchronization signal generating circuits, and generating a synchronization indication signal corresponding to the first node through the one group synchronization signal generating circuit.

11. The synchronization chip according to any one of claims 8 to 10, wherein the N nodes comprise RISC-V cores.