WHAT IS CLAIMED IS:

1. A memory device comprising:

a circuit; and

a wiring,

wherein the circuit comprises a first memory cell and a second memory cell,

wherein the first memory cell comprises a first transistor, a second transistor, and a first capacitor,

wherein one of a source and a drain of the first transistor is electrically connected to a gate of the second transistor and the first capacitor,

wherein a gate insulating layer of the first transistor and a gate insulating layer of the second transistor comprise a first insulating layer,

wherein the second memory cell comprises a third transistor, a fourth transistor, and a second capacitor,

wherein one of a source and a drain of the third transistor is electrically connected to a gate of the fourth transistor and the second capacitor,

wherein the second memory cell is stacked over the first memory cell, and

wherein a gate of the first transistor and a gate of the third transistor comprise a first conductive layer on the first insulating layer, the first conductive layer electrically connected to the wiring.

2. The memory device according to claim 1,

wherein the first transistor further includes a first semiconductor layer in a channel formation region under the first insulating layer,

wherein a gate insulating layer of the third transistor and a gate insulating layer of the fourth transistor comprise a second insulating layer over the first conductive layer, and

wherein the third transistor further includes a second semiconductor layer in a channel formation region over the second insulating layer.

3. A memory device comprising:

a circuit; and

a wiring,

wherein the circuit comprises a first memory cell and a second memory cell,

wherein the first memory cell comprises a first transistor, a second transistor, and a first capacitor,

wherein one of a source and a drain of the first transistor is electrically connected to a gate of the second transistor and the first capacitor,

wherein a gate insulating layer of the first transistor and a gate insulating layer of the second transistor comprise a first insulating layer,

wherein the second memory cell comprises a third transistor, a fourth transistor, and a second capacitor,

wherein one of a source and a drain of the third transistor is electrically connected to a gate of the fourth transistor and the second capacitor,

wherein the second memory cell is stacked over the first memory cell,

wherein a gate of the first transistor and a gate of the third transistor comprise a first conductive layer on the first insulating layer, the first conductive layer electrically connected to the wiring, and

wherein the first transistor, the second transistor, the third transistor, and the fourth transistor each comprise an oxide semiconductor in a channel formation region.

4. The memory device according to claim 3, further comprising:

a row driver; and

a column driver,

wherein the circuit is stacked over the row driver and the column driver, and

wherein the row driver and the column driver each comprise a transistor comprising a material other than the oxide semiconductor in a channel formation region.

5. The memory device according to claim 3, further comprising:

wherein the channel formation region of the first transistor is provided under the first insulating layer,

wherein a gate insulating layer of the third transistor and a gate insulating layer of the fourth transistor comprise a second insulating layer over the first conductive layer, and

wherein the channel formation region of the third transistor is provided over the second insulating layer.

6. The memory device according to claim 1, further comprising a plurality of the circuits, wherein the circuits are stacked.

7. The memory device according to claim 3, further comprising a plurality of the circuits, wherein the circuits are stacked.

8. The memory device according to claim 1, wherein a memory capacity is one terabyte or more.

9. The memory device according to claim 3, wherein a memory capacity is one terabyte or more.

10. An electronic device comprising:
the memory device according to claim 1; and
a host device,
wherein the host device and the memory device are electrically connected to each other.

11. An electronic device comprising:
the memory device according to claim 3; and
a host device,
wherein the host device and the memory device are electrically connected to each other.

12. The memory device according to claim 1, wherein the gate of the second transistor is provided under the first insulating layer.

13. The memory device according to claim 2, wherein the second insulating layer is provided under the gate of the fourth transistor and over the gate of the third transistor.

14. The memory device according to claim 3, wherein the gate of the second transistor is provided under the first insulating layer.

15. The memory device according to claim 5, wherein the second insulating layer is provided under the gate of the fourth transistor and over the gate of the third transistor.