Description

Cross reference to related applications

1. SC-80041 "Horizontal Oscillator", European Application EP—A—0067167.
2. SC-80044 "Horizontal Phase Detector Gain Control", European Application EP—A—0067168.
3. SC-80977 "Horizontal Phase Lock Loop for Television", European Application EP—A—0067201.
4. SC-80978 "Variable Capacitance Circuit", European Application EP—A—0067166.
5. SC-80071 "Linear Full Wave Rectifier Circuit", European Application EP—A—0067163.

Background of the invention

Field of the art:

The present invention relates to television circuits and, more particularly, to a partitioning scheme for a television receiver for providing the video and signal processing circuits on a single large scale integrated circuit.

Description of the prior art:

Since the first television receiver was built comprising discrete circuitry and vacuum tubes television receivers have evolved to the present wherein the television receiver comprises a plurality of integrated circuits in combination with the tuner and high powered portions of the circuit as well as the cathode ray tube (CRT) utilized to provide the television picture.

Generally, contemporary television receivers include a radio frequency (RF) tuner which is coupled to a tuned input of an intermediate frequency (IF) stage the output of which is coupled to both a video processing stage and a signal processing stage wherein the video composite TV signal is processed to drive the cathode ray tube with the output of the signal processing stage being utilized to drive the horizontal and vertical deflection yokes of the television cathode ray tube so that the video information supplied from the video processor is converted to a recognizable picture on the CRT.

Typically, contemporary television receivers require a minimum of four integrated circuits to provide the functions of a basic black and white television receiver. For example, the television receiver can be partitioned in a manner wherein four integrated circuits may be utilized to provide (1) video IF ampilfier and video detection (2) video signal processing (3) horizontal sync information processing and (4) vertical sync information processing.

The aforedescribed combination of multiple integrated circuits results in a problem that is related to all such television receivers which is caused by undesirous signal radiation that occurs to a greater or lesser extent because of the use of external coils in tuned circuits required for detection of the composite TV stereo operating in a high signal environment. For instance, this radiation usually emanates from a portion of the television receiver where the IF signal levels are at the highest: usually at the interface of the video detector stage of the television receiver where the external tuned circuits are utilized for video detection. Another problem with television receivers utilizing multiple integrated circuits is that exact DC signal bias levels must be maintained between each one of the multiple integrated circuits. It is quite difficult to achieve these bias levels and an attempt to so requires external biasing circuitry to be utilized. Still further, the use of multiple integrated circuits can be relatively expensive when compared to a television receiver that required only a single large scale integrated chip to provide the aforementioned functions.

Hence, the present invention is concerned with combining the basic functions of a television receiver, i.e. the IF amplifier/detector stage, video processing and signal processing circuits into a single large scale integrated circuit having optimum partitioning. Such a single integrated circuit can eliminate radiation problems as aforedescribed with elimination of tuned circuits by the use thereof as well as save costs by eliminating the need for mutiple integrated circuits.

Summary of the invention

Accordingly, it is an object of the present invention to provide a large scale integrated circuit television subsystem.

Another object of the present invention is to provide a large scale integrated circuit incorporating the basic functions of a television receiver including the IF amplifier, video detecting and processing, horizontal and vertical processing circuits therefor.

A still further object of the present invention is to provide a large scale integrated circut to be utilized in a television receiver having a horizontal and vertical processing circuit for producing vertical and horizontal sync pulses which are related to each other.

In accordance with the present invention there is provided a television subsystem including a video amplifier circuit, a video detector and signal processor circuit, a signal processing circuit which provides horizontal and vertical sync pulses, a horizontal signal processor circuit, and a vertical signal processor circuit characterized by the aforementioned TV subsystem being integrated in a single integrated circuit having no external tuned circuits coupled to the video detector and signal processor circuit to thereby eliminate signal radiation therefrom and having no need for direct current biasing circuits for maintaining accurate direct current bias levels between the aforementioned integrated TV subsystem as the individual circuits of the integrated TV subsystem are in the same integrated circuit, the video detector of the video detector and signal processor circuit including a video detector circuit comprising a full wave rectifier circuit that is capacitively coupled to the video amplifier to provide a full wave rectified version of said IF signal thereby eliminating the need for said tuned

circuits; the horizontal signal processor circuit being responsive to the horizontal sync pulses and horizontal flyback pulses supplied thereto for producing horizontal deflection output signals at a horizontal line frequency and the vertical signal processor circuit including a countdown circuit which is responsive both to the vertical sync pulses and a clocking signal supplied from the horizontal signal processor circuit for producing vertical deflection output signals.

One feature of the present invention is that the video detector circuit eliminates the use of tuned circuits such that radiation problems which frequently occur in prior art television receivers are eliminated or at least greatly reduced.

Brief description of the drawings

One television subsystem in accordance with the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 is a block diagram illustrating a typical black and white television receiver;

Fig. 2 is a block diagram of the television receiver of an embodiment of the present invention;

Fig. 3 is a block diagram of a vertical countdown circuitry of an embodiment of the present invention; and

Fig. 4 is a schematic diagram of a latch circuit utilized in the vertical countdown circuitry of Fig. 3.

Detailed description of the invention

Turning to Fig. 1, there is shown a typical black and white television receiver which is generally understood to those skilled in the art. Television receiver (10), as shown, comprises a RF tuner section 12 which is coupled to antenna 14 to receive the television composite signal. RF tuner 12 includes a voltage controlled oscillator for converting the composite television signal to an IF frequency which is then applied via a tuned stage to the input of IF amplifier section 16. The output of IF amplifier section 16 is applied to video detector 18 wherein the video information, as well as the vertical and horizontal sync information are detected and separated from the sound information carrying signal. The sound signal is processed through sound processing circuit 20 to be reproduced as audio at speaker 22. The video information is processed through video processing circuit 24 to drive the cathode of cathode ray tube 26 to develop the television picture in conjunction with the vertical and horizontal deflection circuits V and H which surround tube 26. An output is also supplied from video detector 18 to signal processing circuit 28, which as known provides several functional outputs, i.e., gated automatic gain control signals are provided for controlling the gains of the IF amplifier stage 16 and the RF tuner 12 via leads 30 and 32 respectively, also, the horizontal and vertical sync pulses are separated with RF noise spikes eliminated from the sync pulses. The respective pulses are supplied to horizontal and vertical processing circuits 34 and 36. Video processing circuit 24 is shown as receiving contrast and brightness control signals as is understood to vary the signal drive to the cathode of cathode ray tube 26. Video processing circuit 24 also receives a blanking signal from vertical processing circuit 36 to blank the screen of the tube 26 during the vertical flyback period of the television receiver.

Horizontal and vertical processing circuits 34 and 36 each typically include a free running oscillator which may be locked by the respective horizontal and vertical sync pulses supplied thereto for synchronizing the horizontal and vertical scanning to the received video signal. Horizontal scanning information is sampled from the currents introduced through the horizontal deflection coils, H and V, which are positioned about tube 26 in order to maintain synchronization and linearity of drive. The outputs from horizontal and vertical circuits 34 and 36 are supplied to horizontal and vertical output amplifiers 38 and 40 respectively to drive the aforementioned deflection coils.

It should be understood that although the foregoing description refers to a black and white television receiver that those skilled in the art understand that a color receiver is also explained in that only a chroma demodulator and driver stages need be added to the television receiver in a known manner in conjunction with a color cathode ray tube.

Typically, contemporary television receiver 10 comprises a minimum of four integrated circuits (IC's) for providing the IF, video detection, horizontal sync and vertical sync processing. As an example, television receiver 10 can be realized using the following available ICs which are manufactured by Motorola Inc.:

Television circuit	IC
IF Amplifier 16	MC1349/1350
Video Detector and Video Processing Circuits 18 and 24	MC1330/1350
Sound Processing Circuit 20	TDA1190
Signal Processing Circuit 28	MC1344
Horizontal Processing Circuit 34	MC1391
Vertical Processing Circuit 36	MC1393

As mentioned previously, prior art television receivers of the type described above suffer from several disadvantages, i.e. radiation problems and maintenance of accurate dc levels between individual integrated circuits. The present invention relates to specific partitioning of the several individual stages described above into a large scale integrated circuit to eliminate radiation problems generally arising in the video detector portion by eliminating the need for tuned circuits

as well as eliminating the need for several dc biasing circuits for maintaining the dc levels between the individual integrated circuits.

Turning now to Fig. 2, there is shown a large scale integrated television receiver subsystem circuit 50 of the preferred embodiment wherein partitioning of the IF and video processing circuity is accomplished on one single integrated circuit to eliminate the aforementioned problems of the prior art. As illustrated single integrated circuit television receiver subsystem 50 includes video IF amplifier stage 52 to which is supplied the composite television signal at input terminals 52 and 54 from a RF tuner section (not shown). The output of the video IF section is coupled via coupling capacitors 56 and 58 to the input of video detector 60. Coupling capacitors 58 and 56 are integrated on the integrated circuit whereby video detector 60 is ac coupled to video IF amplifier 52. The output at output terminal 62 from video detector is supplied to the sound processor section of the television receiver which is not part of the integrated circuit subsystem 50. Copending European patent application EP—A—0067163, entitled "Linear Full Wave Rectifier Circuit" which is incorporated herein by reference describes a circuit that may be utilized for detecting the video television compsite signal. The composite video information signal appearing at the output of video detector 60 is supplied via lead 64 to video processor circuit 66 and is processed in line manner for prior art processor circuits to provide the luma information to the cathode of the cathode ray tube at output 68 of subsystem circuit 50. It is to be understood that if a colour television receiver is to utilize single subsystem circuit 50 that chroma demodulator and detector circuits would be coupled to output terminal 68 to provide chroma information to a colour tube. The output of video processing circuit 66 is coupled to output 68 through a blank/buffer circuit 70 which receives a blanking input signal via lead 72 to provide the blanking function to the television tube during vertical flyback. Still another output of detector 60 is taken via lead 74 and supplied to noise processing circuit 76 for eliminating noise spikes from the composite video signal appearing at output 74. Noise processing circuit 76 provides the aforementioned function in a known manner wherein the noise spikes are inverted and then added back to the signal for example, to eliminate the same therefrom so that noise spikes will not affect the operation of the sync separator circuit 78. The output of noise processor circuit 76 as well as sync separator 78 and output 80 of video detector 60 is supplied to automatic gain control (AGC) circuit 82. The horizontal flyback signal supplied an input terminal 84 via buffer circuit 86 is also supplied to an input of AGC circuit 82 to develop a gated gain control signal at the outputs of thereof in response to a gain control voltage being developed across an external capacitor 88 supplied to input terminal 90 of the television receiver subsystem 50. AGC circuit 82 operates in a known manner to first vary the gain of the video IF section 52 via lead 92 and then to vary the gain of the RF tuner via lead 94 which is connected at an output pin 96 of television receiver subsystem 50.

The output of noise processor circuit 76 is supplied to sync separator 78 to separate the horizontal and vertical sync pulses are separated from the video composite signal as is well known in the art. The horizontal sync pulses from sync separator 78 and supplied to a horizontal processor circuit 20 via lead 98 with the vertical sync pulse information being supplied to vertical sync circuit 100 via lead 102. Vertical sync circuit 100 may include an integrator circuit.

As illustrated, the horizontal processor portion of television receiver subsystem circuit 50 operates to lock the horizontal flyback signal to the horizontal sync pulse which is in turn locked to the horizontal oscillator 104. An oscillator suitable for use as horizontal oscillator 104 is described in copending European patent application EP—A—0067167, entitled "Horizontal Oscillator", and incorporated herein by reference operates at a frequency equal to twice the horizontal line frequency, i.e., 31.5 kHz. In the present embodiment, the horizontal processing circuit besides including horizontal oscillator 104, comprises a phase lock loop circuit comprising two loops. The first loop includes oscillator 104 which is a free running oscillator line the output thereof being provided to a slicer and divide by two circuit 106. The output of slicer circuit 106 is provided to a first phase detector 108 which is gated by the horizontal sync pulses provided from sync separator 78 via lead 98. The output of phase detector 108 is provided at an output 110 to a low pass filter (not shown) and is returned to the input of the horizontal oscillator 104 at an input pin 112. In this manner, the frequency of the horizontal oscillator 104 is varied such that the horizontal sync pulses are centered about the trailing edges of the output pulses of the horizontal oscillator 104. The second loop of the two-loop horizontal phase lock loop circuit includes oscillator 104, slicer/divide by two circuit 106, and a second phase detector 114 which is gated by the flyback pulses from the horizontal deflection circuit of the television receiver and supplied at input terminal 84 through flyback buffer 86. The output of phase detector 114 is supplied at an output 116 to a low pass filter which may be, as shown, capacitor 118 to bias a variable slicer/divide by two circuit 120 which also receives the horizontal oscillator pulses via lead 122. In this manner, the horizontal flyback pulse is centered about a point on the output of the oscillator such that the horizontal flyback pulses are locked with respect to the horizontal sync pulses to the horizontal oscillator. A detailed description of a horizontal processor circuit that may be utilized in the present invention is provided in aforereferenced copending European patent application EP—A—0067201, entitled "Horizontal Phase Lock Loop for Television" which is incorporated herein by reference. The output of variable slicer 120 supplied through

a horizontal buffer circuit 124 to output pin 126. As understood, the output from the horizontal processor circuit, at output pin 126, is supplied to a horizontal driver amplifier to drive the horizontal deflection coils of the cathode ray tube of the television receiver. Phase detector 108 is shown as also receiving an input control signal via lead 128 from a window control circuit 130. As is fully explained in copending European patent application EP—A—0067168, entitled "Horizontal Phase Detector Gain Control", and incorporated herein by reference, the gain of the phase detector 108 is varied by this control signal supplied from window control circuit 130 in accordance with the television receiver being either in sync or not with the television composite signal. Hence, if the television receiver is in sync the gain of phase detector 108 is at a nominal value and is then increased if the television is not in sync to the incoming composite television signal, this increases the bandwidth of the phased locked loop to effect a faster pull-in of the horizontal sync pulses as is understood. An output of horizontal oscillator 104 is taken via lead 131 and is supplied to a vertical countdown circuit 132. Vertical sync pulses are also supplied to the vertical processor circuit from vertical sync circuit 100. As will be fully explained hereinafter, the vertical sync pulses are utilized to reset vertical countdown circuit 132, a divide by 525 counter, such that in response to the input pulses supplied from the horizontal oscillator 104, a vertical flyback pulse is derived once each frame, as is required to sync the vertical picture scanning to the received video signal. Vertical countdown circuit 132 also supplies the aforementioned blanking signal via lead 72 to blanking buffer 70. The output of the vertical countdown circuit 132 is provided to vertical scan circuit 134. The output of vertical countdown circuit 132 is essentially the vertical sync pulse which is then utilized to generate a ramp signal across the RC combination connected at pin 136 to derive the vertical flyback pulse via vertical preamplifier 138 to the vertical deflection coils of the tube at output 140. A feedback signal generated through the vertical deflection coils of the tube is supplied at input pin 142 to an input of vertical preamp 138 to insure tracking of the vertical flyback pulse.

Turning to Figs. 3 and 4, the combined operation of vertical countdown circuit 32 and window control circuit 130 can be explained. Window control circuit 130 is fully discussed in the aforereferenced application EP—A—0067168, entitled, "'Horizontal Phase Detector Gain Control" with respect to generating a gain control signal for varying the gain of phase detector 108 when the television receiver incorporating the present invention is out of sync. The foregoing patent application is incorporated herein by reference. Briefly, the output pulses of horizontal oscillator 104 are supplied to the input of countdown circuit 132 to initiate vertical countdown. Vertical countdown circuit 132 comprises a ten stage counter 144 as understood. The horizontal oscillator clock pulses are divided by 525 by the counter to provide a decode signal once each frame of the television picture to coincide with the vertical sync pulse supplied from vertical sync circuit 100. Vertical countdown circuit 132 includes a reset circuit 150 for among other things providing a reset pulse via lead 146 to reset counter 144 on the occurrence of a vertical sync pulse.

In normal operation, with the television receiver in sync, the vertical sync pulse is supplied to a plurality of serially connected logic gate inverters 150a at the input of reset circuit 150. These gates may be enabled at the 514th count of counter 144 by gate 152 to allow the sync pulse to pass to latch portion 150b of reset circuit 150. The latch portion provides an output both at the input of reset portion 150c of reset circuit 150 and to the input of vertical scan circuit 134 to initiate the vertical flyback period as preivously discussed. The structure of the latch circuit is shown in Fig. 4 and includes a pair of integrated injection logic (I^2L) NAND gates as shown. At a predetermined level of the ramp signal generated at terminal 136 a stop signal is initiated from vertical scan circuit 134 via lead 154 to put latch portion 150b in its latched state to thereby inhibit the input to vertical scan circuit 134 as well as to reset reset portion 150c. Therefore, in addition to initiating the vertical flyback period, the horizontal sync pulse produces a reset signal to reset counter 144. The reset portion of reset circuit 150 may be a D-type flip flop circuit.

Between the 524th and 526th counts of the counter a narrow window pulse is produced via output lead 156 to the input of coincidence detector 148 of window control circuit 130. If coincidence occurs during this narrow window with the reset signals applied via lead 158, coincidence detector 148 maintains the nominal gain of phase detector 108 and gate 152 is enabled to in turn enable the gates of circuit 150. Thus, a narrow window is established between counts 514 to 526 within which coincidence of the vertical sync pulse must occur. If vertical sync is lost for one reason or another such that a vertical sync pulse does not occur during this narrow window pulse, counter 144 provides a decode signal at count 526 through "OR" gate 160 to produce a reset pulse to the counter. However, after eight missing sync pulses window control circuit 130 defaults to a wide window mode to vary the gain of phase detector 108 as well as to open the period that the gates of reset circuit 150 are enabled. In this wide window mode, gate 152 is disabled by coincidence detector 148 which therefore enables wide window latch 162 to enable the gates of reset counter 150 at the 86th count from counter 144. Simultaneously, gate 160 is enabled to provide a decode signal at the 546th count. Thus, a wide window pulse is initiated to occur between the 86th and 546th count. As soon as a vertical sync pulse is acquired during the wide window mode, window control circuit 130 reverts back to the narrow window mode of

operation. Hence, during normal operating conditions a narrow window mode of operation is established in television subsystem 50 to inhibit noise interfering with vertical synchronization of the television receiver with a wide window mode being defaulted to when vertical sync pulses are lost for one reason or another to thereby allow ...t acquisition thereof.

Thus, what has been described is a single chip integrated circuit that will perform the electronic functions of a monochrome television receiver with the exception of the tuner, sound channel and power output stages. It is to be understood that the aforedescribed single chip integrated circuit can be utilized in conjunction with a chrome demodulator detector stage to provide a color television receiver.

Claims

1. A television (TV) subsystem including a video IF amplifier circuit (16), a video detector and ...nal processor circuit (18), a signal processing circuit (28) which provides horizontal and vertical sync pulses, a horizontal signal processor circuit (34), and a vertical signal processor circuit (36) characterized by the aforementioned TV subsystem being integrated in a single integrated circuit having no external tuned circuits coupled to the video detector and signal processor circuit to thereby eliminate signal radiation therefrom and having no need for direct current biasing circuits for maintaining accurate direct current bias levels between the aforementioned integrated TV subsystem as the individual circuits of the integrated TV subsystem are in the same integrated circuit, the video detector of the video detector and signal processor circuit (18) including a video detector circuit (60) comprising a full wave rectifier circuit that is capacitively coupled to the video IF amplifier to provide a full wave rectified version of said IF signal thereby eliminating the need for said tuned circuits; the horizontal signal processor ci...uit being responsive to the horizontal sync p...es and horizontal flyback pulses supplied thereto for producing horizontal deflection output signals at a horizontal line frequency; and the vertical signal processor circuit including a countdown circuit (132) which is responsive both to the vertical sync pulses and a clocking signal supplied from the horizontal signal processor circuit for producing vertical deflection output signals.

2. The TV integrated subsystem of claim 1 characterized by said clocking signal occurs at twice the horizontal line frequency; and said horizontal signal processor circuit includes a two loop phase locked loop such that said horizontal flyback pulses are locked in relation to said horizontal sync pulses; said phase locked loop including a single free running oscillator (104) operating at twice said horizontal line frequency and having an output supplied to said countdown circuit (132), a first phase detector (108) coupled with said oscillator to lock the frequency of the ...atter to the horizontal sync pulses and a second phase detector (114) coupled with said oscillator and being responsive to the horizontal flyback pulses for correcting the phasing of the horizontal flyback pulses with respect to said oscillator such that said frequency of said oscillator is varied wherein the output therefrom occurs in relation to the horizontal sync pulses.

3. The TV integrated subsystem of claim 2 characterized by said vertical signal processor further including a window control circuit (130); and wherein said countdown circuit (132) being coupled with said window control circuit for receiving said vertical sync pulses therefrom and being responsive to both said vertical sync pulses and said clocking signals wherein the TV integrated subsystem operates in a vertical narrow window mode when coincidence occurs between said vertical sync pulses and a reset window pulse produced by said countdown circuit, the subsystem operating in a wide window mode in the absence of said coincidence until such time said coincidence is re-established, the gain of one of said two loops of said horizontal phase locked loop being varied in accordance with each mode of operation.

4. A television receiver including the television subsystem according to any of the preceding claims.

Patentansprüche

1. Fernseh-(TV-)Untersystem, enthaltend eine Video-ZF-Verstärkerschaltung (16), eine Videodetektor- und Signalprozessorschaltung (18), eine Signalprozessorschaltung (28), die Horizontal- und Vertikal-Synchronimpulse Liefert, eine Horizontalsignalprozessorschaltung (34) und eine Vertikalprozessorschaltung (36), dadurch gekennzeichnet, daß das vorgenannte TV-Untersystem in einer einzigen integrierten Schaltung integriert ist, die keine äußeren abgestimmten Kreise enthält, die mit dem Videodetektor- und Signalprozessorschaltung verbunden sind, um dadurch eine Signalabstrahlung davon zu unterbinden, und die keine Notwendigkeit für Gleichstromvorspannschaltungen zur Aufrechterhaltung exakter Gleichstromvorspannungspegel zwischen dem vorgenannten integrierten TV-Untersystem aufweist, da die einzelnen Schaltungen des integrierten TV-Untersystems in derselben integrierten Schaltung sind, wobei der Videodetektor der Videodetektor- und Signalprozessorschaltung (18) eine Videodetektorschaltung (60) enthält, die eine Vollweggleichrichterschaltung aufweist, die kapazitiv mit dem Video-ZF-Verstärker verbunden ist, um eine Vollweg-gleichgerichtete Version des ZF-Signals abzugeben, um dadurch die Notwendigkeit für die genannten abgestimmten Kreise zu beseitigen; wobei die Horizontalsignalprozessorschaltung auf die Horizontalsynchronimpulse und die Horizontal-Rücklaufimpulse, die ihr zugeführt sind, anspricht, um Horizontalablenkungsausgangssignale mit einer Horizontalzeilenfrequenz zu erzeugen; und die Vertikalprozessorschaltung eine Abwärtszählschaltung (132) enthält, die

operation. Hence, during normal operating conditions a narrow window mode of operation is established in television subsystem 50 to inhibit noise interfering with vertical synchronization of the television receiver with a wide window mode being defaulted to when vertical sync pulses are lost for one reason or another to thereby allow t acquisition thereof.

Thus, what has been described is a single chip integrated circuit that will perform the electronic functions of a monochrome television receiver with the exception of the tuner, sound channel and power output stages. It is to be understood that the aforedescribed single chip integrated circuit can be utilized in conjunction with a chrome demodulator detector stage to provide a color television receiver.

Claims

1. A television (TV) subsystem including a video IF amplifier circuit (16), a video detector and jnal processor circuit (18), a signal processing circuit (28) which provides horizontal and vertical sync pulses, a horizontal signal processor circuit (34), and a vertical signal processor circuit (36) characterized by the aforementioned TV subsystem being integrated in a single integrated circuit having no external tuned circuits coupled to the video detector and signal processor circuit to thereby eliminate signal radiation therefrom and having no need for direct current biasing circuits for maintaining accurate direct current bias levels between the aforementioned integrated TV subsystem as the individual circuits of the integrated TV subsystem are in the same integrated circuit, the video detector of the video detector and signal processor circuit (18) including a video detector circuit (60) comprising a full wave rectifier circuit that is capacitively coupled to the video IF amplifier to provide a full wave rectified version of said IF signal thereby eliminating the need for said tuned circuits; the horizontal signal processor circuit being responsive to the horizontal sync pulses and horizontal flyback pulses supplied thereto for producing horizontal deflection output signals at a horizontal line frequency; and the vertical signal processor circuit including a countdown circuit (132) which is responsive both to the vertical sync pulses and a clocking signal supplied from the horizontal signal processor circuit for producing vertical deflection output signals.

2. The TV integrated subsystem of claim 1 characterized by said clocking signal occurs at twice the horizontal line frequency; and said horizontal signal processor circuit includes a two loop phase locked loop such that said horizontal flyback pulses are locked in relation to said horizontal sync pulses; said phase locked loop including a single free running oscillator (104) operating at twice said horizontal line frequency and having an output supplied to said countdown circuit (132), a first phase detector (108) coupled with said oscillator to lock the frequency of the latter to the horizontal sync pulses and a second phase detector (114) coupled with said oscillator and being responsive to the horizontal flyback pulses for correcting the phasing of the horizontal flyback pulses with respect to said oscillator such that said frequency of said oscillator is varied wherein the output therefrom occurs in relation to the horizontal sync pulses.

3. The TV integrated subsystem of claim 2 characterized by said vertical signal processor further including a window control circuit (130); and wherein said countdown circuit (132) being coupled with said window control circuit for receiving said vertical sync pulses therefrom and being responsive to both said vertical sync pulses and said clocking signals wherein the TV integrated subsystem operates in a vertical narrow window mode when coincidence occurs between said vertical sync pulses and a reset window pulse produced by said countdown circuit, the subsystem operating in a wide window mode in the absence of said coincidence until such time said coincidence is re-established, the gain of one of said two loops of said horizontal phase locked loop being varied in accordance with each mode of operation.

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sowohl auf die Vertikalsynchronimpule als auch auf ein Taktsignal anspricht, das von der Horizontalsignalprozessorschaltung zugeführt ist, um Vertikalablenkausgangssignale zu erzeugen.

2. Integriertes TV-Untersystem nach Anspruch 1, dadurch gekennzeichnet, daß das genannte Taktsignal mit dem Zweifachen der Horizontalzeilenfrequenz auftritt; und die Horizontalsignalprozessorschaltung eine zweischleifige Phasenverriegelungsschleife enthält, so daß die Horizontal-Rücklaufimpulse in bezug auf die Horizontalsynchronimpulse verriegelt werden; wobei die genannte Phasenverriegelungsschleife einen einzigen freilaufenden Oszillator (104) enthält, der mit dem Zweifachen der Horizontalzeilenfrequenz arbeitet und einen Ausgang hat, der der Abwärtszählschaltung (132) zugeführt ist, mit einem ersten Phasendetektor (108), der mit dem Oszillator verbunden ist, um die Frequenz desselben mit den Horizontalsynchronimpulsen zu verriegeln, und einem zweiten Phasendetektor (114), der mit dem Oszillator verbunden ist und auf die Horizontal-Rücklaufimpulse anspricht, um die Phasenlage der Horizontal-Rücklaufimpulse in bezug auf den Oszillator zu korrigieren, so daß die Frequenz des Oszillators variiert, wobei der Ausgang desselben in bezug auf die Horizontalsynchronimpulse auftritt.

3. Integriertes TV-Untersystem nach Anspruch 2, dadurch geeknnzeichnet, daß der genannte Vertikalsignalprozessor weiterhin eine Fensterstuerschaltung (130) enthält und wobei die Abwärtszählschaltung (132) mit der Fenstersteuerschaltung verbunden ist, um die Vertikalsynchronimpulse davon aufzunehmen und die sowohl auf die Vertikalsynchronimpulse als auch auf die Taktsignale anspricht, wobei das integrierte TV-Untersystem in einer Vertikal-Schmalfensterbetriebsart arbeitet, wenn keine Koinzidenz zwischen den Vertikalsynchronimpulsen und einem Rücksetzfensterimpulse auftritt, der von der Abwärtszählschaltung erzeugt wird, und das Untersystem in einer Breitfensterbetriebsart bei Abwesenheit der genannten Koinzidenz solange arbeitet, bis die genannte Koinzidenz wiederhergestellt ist, wobei die Verstärkung von einer der zwei Schleifen der genannten Horizontal-Phasenverriegelungsschleife in Übereinstimmung mit jeder Betriebsart veriiert wird.

4. Fernsehempfänger, der das Fernsehuntersystem nach einem der vorhergehenden Ansprüche enthält.

Revendications

1. Un sous-système de télévision (TV) comprenant un circuit amplificateur FI vidéo (16), un circuit de détecteur et de traitement de signal vidéo (18), un circuit de traitement de signal (28) qui produit des impulsions de synchronisation horizontale et verticale, un circuit de traitement de signal horizontal (34) et un circuit de traitement de signal vertical (36), caractérisé par le fait que le sous-système de TV précité est intégré dans un seul circuit intégré ne comportant aucun circuit accordé externe connecté au circuit de détecteur et de traitement de signal vidéo, pour éliminer ainsi un rayonnement de signal à partir de ce circuit, et ne nécessitant aucun circuit de polarisation en courant continu pour maintenir des niveaux de polarisation en courant continu précis dans le sous-système de TV intégré précité, du fait que les circuits individuels du sous-système de TV intégré se trouvent dans le même circuit intégré, le détecteur vidéo du circuit de détecteur et de traitement de signal vidéo (18) comprenant un circuit détecteur vidéo (60) qui comprend un circuit redresseur à double alternance qui est en couplage capacitif avec l'amplificateur FI vidéo, pour fournir une version redressée à double alternance du signal FI, afin d'éliminer la nécessité des circuits accordés précités; le circuit de traitement de signal horizontal réagissant aux impulsions de synchronisation horizontale et à des impulsions de retour de balayage horizontal qui lui sont appliquées, en produisant des signaux de sortie de déflexion horizontale à une fréquence de lignes horizontales; et le circuit de traitement de signal vertical comprenant un circuit de comptage (132) qui réagit à la fois aux impulsions de synchronisation verticale et à un signal d'horloge provenant du circuit de traitement de signal horizontal, de façon à produire des signaux de sortie de déflexion verticale.

2. Le sous-système intégré de TV de la revendication 1, caractérisé en ce que le signal d'horloge apparaît au double de la fréquence de lignes horizontales; et le circuit de traitement de signal horizontal comprend une double boucle de verrouillage de phase, de façon que les impulsions de retour de balayage horizontal soient verrouillées sur les impulsions de synchronization horizontale; cette boucle de verrouillage de phase comprenant un seul oscillateur libre (104), fonctionnant au double de la fréquence de lignes horizontales et ayant un signal de sortie qui est appliqué au circuit de comptage (132), un premier détecteur de phase (108) connecté à l'oscillateur pour verrouiller la fréquence de ce dernier sur les impulsions de synchronisation horizontale, et un second détecteur de phase (114) qui est connecté à l'oscillateur et qui réagit aux impulsions de retour de balayage horizontal en corrigeant la phase des impulsions de retour de balayage horizontal, par rapport à l'oscillateur, de façon que la fréquence de l'oscillateur varie pour que ou signal de sortie apparaisse en relation avec les impulsions de synchronisation horizontale.

3. Le sous-système intégré de TV de la revendication 2, caractérisé en ce que le circuit de traitement de signal vertical comprend en outre un circuit de commande à fenêtre (130); et en ce que le circuit de comptage (132) est connecté au circuit de commande à fenêtre de façon à recevoir les impulsions de synchronisation verticale provenant de ce dernier, et il réagit à le fois à ces impulsions de synchronisation verticale et aux signaux d'horloge, le sous-système intégré de TV fonctionne dans un mode à fenêtre verticale étroite en cas de coïncidence entre les impulsions

de synchronization verticale et une impulsion de fenêtre de restauration qui est produite par le circuit de comptage, et le sous-système fonctionne dans un mode à fenêtre large en l'absence de cette coïncidence, jusqu'au moment où la coïncidence est rétablie, le gain de l'une des deux boucles de la boucle de verrouillage de phase horizontale étant modifié conformément à chaque mode de fonctionnement.

4. Un récepteur de télévision comprenant le sous-système de télévision conforme à l'une quelconque des revendications précédentes.