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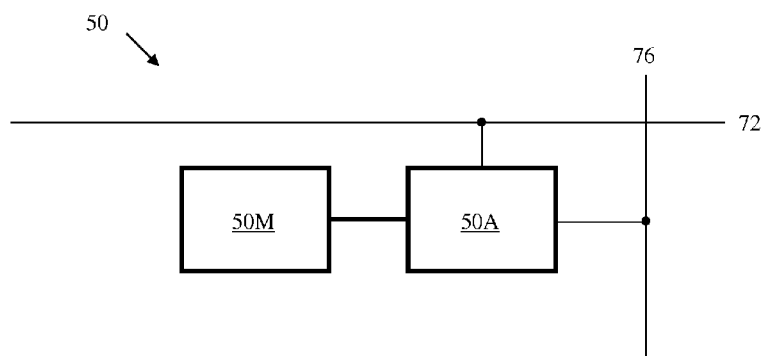


FIG. 1A

(57) Abstract: Semiconductor memory cells, array and methods of operating are disclosed. In one instance, a memory cell includes a bi-stable floating body transistor and an access device; wherein the bi-stable floating body transistor and the access device are electrically connected in series.