

ABSTRACT OF THE DISCLOSURE

A method of operating a memory device including row pins and column pins includes receiving a first active command through the row pins during a first 1.5 cycles of a clock signal, receiving a first read command or a first write command through the column pins during a first 1 cycle of the clock signal, receiving a first precharge command through the row pins during a first 0.5 cycle of the clock signal corresponding to a rising edge of the clock signal, receiving a second active command through the row pins during a second 1.5 cycles of the clock signal, receiving a second read command or a second write command through the column pins during a second 1 cycle of the clock signal, and receiving a second precharge command through the row pins during a second 0.5 cycle of the clock signal corresponding to a falling edge of the clock signal.

FIG. 5