

ABSTRACT

A memory device includes a memory cell array, an information register and a prefetch circuit. The memory cell array stores a valid data array, a base array and a target data array, where the valid data array includes valid elements among elements of first data, the base array includes position elements indicating position values corresponding to the valid elements and the target data array includes target elements of second data corresponding to the position values. The information register stores indirect memory access information including a start address of the target data array and a unit size of the target elements. The prefetch circuit prefetches, based on the indirect memory access information, the target elements corresponding to the position elements that are read from the memory cell array.

FIG. 1