**Abstract**

A semiconductor device has a vertical interconnect structure with a first conductive pillar and a first encapsulant deposited around the first conductive pillar. A second conductive pillar is formed over the first conductive pillar. A second encapsulant is deposited around the second conductive pillar. Additional conductive pillars and encapsulant deposited around the conductive pillars can be formed to extend a height of the vertical interconnect structure. The first conductive pillar can have an angled sidewall or a vertical sidewall. The second conductive pillar can have an angled sidewall or a vertical sidewall. A surface of the second conductive pillar as exposed from the second encapsulant is planarized. A width of the first conductive pillar is different from a width of the second conductive pillar. A pitch of a sidewall of the first conductive pillar is different from a pitch of a sidewall of the second conductive pillar.

(Fig.2t)