SPACER-LESS LOW-K DIELECTRIC PROCESSES

Abstract

A first example embodiment provides a method of removing first spacers from gates and incorporating a low –k material into the ILD layer to increase device performance. A second example embodiment comprises replacing the first spacers after silicidation with low-k spacers. This serves to reduce the parasitic capacitances. Also, by implementing the low-k spacers only after silicidation, the embodiments' low-k spacers are not compromised by multiple high dose ion implantations and resist strip steps. The example embodiments can improve device performance, such as the performance of a rim oscillator.

Figure 7A