

MOSFET WITH SUBSTRATE SOURCE CONTACT

ABSTRACT OF THE DISCLOSURE

5 A MOSFET (90,105,170) having a back-side source contact
 (94,169) and top-side gate (104,166) and drain contacts
 (98,168) is provided by a structure comprising superposed N⁺
 (97,136), N⁻ (96,132), P⁻ (95,128), N⁺ (92,120) regions
 arranged between top (99,137) and bottom (93,121) surfaces
10 of the semiconductor die (90,105,170). In a preferred
 implementation, two trenches (100,108) (148,149) are etched
 from the top surface (99,137) to the P⁻ (95,128), N⁺
 (92,120) interface. A buried P⁻ (95,128), N⁺ (92,120) short
 (110,162) is provided in one trench (108,148) and a gate
15 dielectric (102,160) and gate electrode (104,166) are
 provided over the sidewall P⁻ (95,128) region exposed in the
 other trench (100,149). This creates a vertical MOSFET
 (170) in which the N⁺ substrate (92,120) forms the source
 region shorted to the P⁻ body region (95,128) in which the
20 channel (106) is created by the gate (104,166). Superior
 performance is obtained in RF grounded-source circuit
 applications.

Fig. 7 accompanies this abstract.

This Sheet Has Been Replaced

