Claims

What is claimed:

1. A semiconductor device, comprising:

a semiconductor wafer including a plurality of semiconductor die separated by a saw street;

a first conductive layer formed over the semiconductor die;

a first insulating layer including a non-planar surface formed over the semiconductor ~~wafer~~die and first conductive layer; and

a protective layer ~~including a planar surface formed over the first insulating layer; and~~

~~an encapsulant deposited over the semiconductor die~~ including a planar surface formed over the saw street and the first insulating layer and covering the first conductive layer.

2. The semiconductor device of claim 1, further including a trench formed in the protective layer over the saw street.

3. The semiconductor device of claim 2, further including a second conductive layer formed over the ~~trench~~ saw street between adjacent semiconductor die.

4. The semiconductor device of claim 1, further including a trench comprising a plurality of notches formed in the protective layer over the saw street.

~~5. The semiconductor device of claim 1, wherein the encapsulant is planarized with a surface of the semiconductor die.~~

~~6. The semiconductor device of claim 1, further including an interconnect structure formed over the semiconductor die and encapsulant.~~

~~7~~5. A semiconductor device, comprising:

a semiconductor wafer including a plurality of semiconductor die separated by a saw street;

a first insulating layer formed over the semiconductor wafer; and

a protective layer formed over the saw street and first insulating layer~~; and~~

~~an encapsulant deposited over the semiconductor die~~.

~~8~~6. The semiconductor device of claim ~~7~~5, wherein the first insulating layer has a non-planar surface and the protective layer has a planar surface.

~~9~~7. The semiconductor device of claim ~~7~~5, further including a trench formed in the protective layer over the saw street.

~~10~~8. The semiconductor device of claim ~~7~~5, wherein the protective layer is formed over an entire surface of the semiconductor wafer.

~~11. The semiconductor device of claim 7, wherein the encapsulant is planarized with a surface of the semiconductor die.~~

~~12. The semiconductor device of claim 7, further including a channel formed in the encapsulant outside a footprint of the semiconductor die.~~

~~13. The semiconductor device of claim 7, further including an interconnect structure formed over the semiconductor die and encapsulant.~~

~~14~~9. A semiconductor device, comprising:

a semiconductor die;

a first insulating layer including a non-planar surface formed over the semiconductor die;

~~a protective layer including a planar surface formed over the first insulating layer; and~~

an encapsulant deposited over the semiconductor die; and

a first channel formed in the encapsulant adjacent to the semiconductor die.

1~~5~~0. The semiconductor device of claim ~~14~~9, wherein the encapsulant is planarized with a surface of the semiconductor die.

1~~6~~1. The semiconductor device of claim ~~14~~9, further including a second insulating layer disposed in the first channel ~~formed in the encapsulant outside a footprint of the semiconductor die~~.

1~~7~~2. The semiconductor device of claim 1~~4~~1, further including a second channel formed in the ~~encapsulant adjacent to the semiconductor die~~ second insulating layer.

1~~8~~3. The semiconductor device of claim ~~14~~9, further including an interconnect structure formed over the semiconductor die and encapsulant.

19~~4~~. The semiconductor device of claim 18~~3~~, wherein the interconnect structure includes:

a second insulating layer formed over the encapsulant and first insulating layer;

a conductive layer formed over the second insulating layer; and

a third insulating layer formed over the second insulating layer and conductive layer.

20~~15~~. A semiconductor device, comprising:

a semiconductor die;

a first insulating layer formed over the semiconductor die;

a protective layer formed over the first insulating layer; and

an encapsulant deposited over the semiconductor die coplanar with the protective layer.

21~~16~~. The semiconductor device of claim 20~~15~~, wherein the first insulating layer has a non-planar surface.

22~~17~~. The semiconductor device of claim 20~~15~~, wherein the protective layer has a planar surface.

23~~18~~. The semiconductor device of claim 20~~15~~, wherein the encapsulant is planarized with a surface of the semiconductor die.

24~~19~~. The semiconductor device of claim 20~~15~~, further including a channel formed in the encapsulant outside a footprint of the semiconductor die.

~~25. The semiconductor device of claim 20, further including an interconnect structure formed over the semiconductor die and encapsulant.~~

20. The semiconductor device of claim 2, wherein a width of the trench is less than a width of the saw street.

21. The semiconductor device of claim 3, wherein a width of the trench is less than a width of the conductive layer.

22. The semiconductor device of claim 7, wherein a width of the trench is less than a width of the saw street.

23. The semiconductor device of claim 7, further including a conductive layer formed over the saw street between adjacent semiconductor die.

24. The semiconductor device of claim 23, wherein a width of the trench is less than a width of the conductive layer.