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VERTICAL SOURCE/DRAIN CONTACT SEMICONDUCTOR

TECHNICAL FIELD

The present invention relates generally to semiconductor devices, and more particularly to silicon on insulator transistors.

BACKGROUND ART

Semiconductor devices such as transistors, resistors, capacitors, and other circuit elements, are formed in and upon semiconductor substrates. These circuit elements are interconnected by contacts and vias, which connect to patterned conductor layers which are separated by various dielectric layers.

A critical objective of the semiconductor industry has been to continually decrease the size of semiconductor devices to increase performance and reduce cost.

The ability to reduce performance degrading parasitic capacitances resulting from diffusion of junction dopants into semiconductor substrates has been accomplished through the use of silicon on insulator (SOI) technology. The SOI technology consists of forming the desired semiconductor devices in a layer of silicon, which overlies an insulator layer deposited on a conventional semiconductor substrate.

As semiconductor technology has advanced, there has been a continuing concentration on reducing the size of the semiconductor devices to allow for increased levels of circuit integration, improved performance, and higher density.

However, when the length and width of a semiconductor device are reduced, the length and width of the contacts connected to the semiconductor device must also be reduced. When the length and width of the contacts are reduced, the cross-sectional area is reduced by the square of the length or width and the resistance generally increases by the square (power of 2). The industry is currently reaching the point where the size is so small that the relative resistance is so high as to render connection to small devices impossible.

As devices continue to be reduced in size, it is clear that a breakthrough solution to this problem is required for continued success in reducing semiconductor device

size and thus increasing device integration, performance, and function while at the same time reducing cost.

DISCLOSURE OF THE INVENTION

The present invention provides a semiconductor device and manufacturing process therefor in which vertical trenches are formed in the semiconductor or the silicon on insulator substrate adjacent to the sides of the semiconductor gate to expose the source/drain junctions. The contacts having inwardly curved cross-sectional widths in the semiconductor substrate connect vertically to the exposed source/drain junctions either directly or through salicided contact areas to provide a smaller semiconductor device (transistor) footprint.

The present invention further provides a semiconductor device and manufacturing process therefor in which vertical trenches are formed in the semiconductor or the silicon on insulator substrate adjacent to the sides of the semiconductor gate to expose the source/drain junctions. The contacts having inwardly curved cross-sectional widths in the semiconductor substrate connect vertically to the exposed source/drain junctions either directly or through salicided contact areas to provide a contact to silicon connection.

The present invention further provides a semiconductor device and manufacturing process therefor in which angled implantation of dopant followed by formation of vertical trenches, which are also implanted with dopant. A rapid thermal anneal forms source/drain extension junctions in the semiconductor or the silicon on insulator substrate which are below the surface thereof to provide reduced junction parasitic capacitance.

The present invention further provides a semiconductor device and manufacturing process therefor in which vertical trenches are formed in the semiconductor or the silicon on insulator substrate adjacent to the sides of the semiconductor gate to expose the source/drain junctions. The contacts having inwardly curved cross-sectional widths in the semiconductor substrate connect vertically to the exposed source/drain junctions either directly or through salicided contact areas to provide increased area vertical electrical connections between the contact and the silicon.

The present invention further provides a semiconductor device and manufacturing process therefor in which vertical trenches are formed in the semiconductor or the silicon on insulator substrate adjacent to the sides of the semiconductor gate to expose the source/drain junctions. The contacts having inwardly curved cross-sectional widths in the semiconductor substrate connect vertically to the exposed source/drain junctions either directly or through salicided contact areas to provide a new method of forming contact to silicon connections.

The above and additional advantages of the present invention will become apparent to those skilled in the art from a reading of the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross section of a semiconductor device in an initial stage of formation,

FIG. 2 is the structure of FIG. 1 after a sacrificial layer (not shown) is deposited on the semiconductor layer and patterned for the formation and growth of an insulator layer;

FIG. 3 is the structure of FIG. 2 after successive depositions of a gate dielectric, a floating gate electrode, an inner gate layer, and a control gate electrode.

FIG. 4 is the structure of FIG. 3 after a photoresist is deposited, patterned, and developed in a conventional manner followed by an etch process to remove unprotected portions of the layers above the substrate to form a gate stack;

FIG. 5 is the structure of FIG. 4 undergoing source/drain (S/D) extension junction implantation to form S/D extension junctions;

FIG. 6 is the structure of FIG. 5 having a barrier layer and a spacer layer deposited thereon;

FIG. 7 is the structure of FIG. 6 after an anisotropic etch to remove portions of the spacer layer and a subsequent etch to remove portions of the barrier layer to expose the SOI layer and to form a sidewall spacer;

FIG. 8 is the structure of FIG. 7 during a low-angle, four-quadrant implantation;

FIG. 9 is the structure of FIG. 8 after a rapid thermal anneal (RTA) which causes enhanced thermal diffusion (TED) of the S/D junctions and the S/D extension junctions;

FIG. 10 is the structure of FIG. 9 after the deposition, patterning, developing, and etching of a contact interlayer dielectric (ILD) and a channel layer ILD;

FIG. 11 is a top view of the structure of FIG. 10;

FIG. 12 is an alternate embodiment to the structure shown in FIG. 10; and

FIG. 13 is a top view of the structure of FIG. 12.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention as hereinafter described is embodied in a silicon on insulator (SOI) transistor device, but it should be understood that it is applicable to many different semiconductor devices which require reduced length and widths without a corresponding decrease in the contact area.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as just defined. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over", and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

Referring now to FIG. 1, therein is shown a semiconductor device 10 in an initial stage of formation. A semiconductor substrate, such as a silicon substrate 12, has an insulator layer, such as a silicon oxide layer 14, and a second semiconductor substrate, such as a doped silicon on insulator (SOI) layer 16, successively deposited thereon.

Referring now to FIG. 2, therein is shown the structure of FIG. 1 after a sacrificial layer (not shown) is deposited on the SOI layer 16 and patterned for the formation and growth of an insulator layer, a field oxide 18. The sacrificial layer is removed and a chemical mechanical polishing process planarizes the field oxide and the SOI layer 16.

Chemical-mechanical polishing (referred to as "CMP") typically involves mounting a wafer face down on a holder and rotating the wafer face under pressure

against a polishing pad mounted on a polishing platen, which in turn is rotating or is in orbital state. A slurry containing a chemical that chemically interacts with the facing wafer layer and an abrasive that physically removes that layer is flowed between the wafer and the polishing pad or on the pad near the wafer. A combination of the chemical reaction between the slurry and the layer being polished and the mechanical interaction between abrasives within the slurry and the layer being polished cause the planarization of the layer. During integrated circuit fabrication, this technique is commonly applied to planarize various wafer layers, such as dielectric layers, metallization, etc.

Referring now to FIG. 3, therein is shown the structure of FIG. 2 after successive depositions of a gate dielectric, a floating gate electrode, an inner gate layer, and a control gate electrode. In the preferred embodiment, the gate dielectric layer is a gate oxide (GOX) layer 20, the floating gate electrode is a polysilicon (Si) layer 22, the inner gate layer is a tungsten (W) layer 24, and the control gate electrode is a silicon oxynitride (SiON) layer 26.

Referring now to FIG. 4, therein is shown the structure of FIG. 3 after a photoresist (not shown) is deposited, patterned, and developed in a conventional manner followed by an etch process to remove unprotected portions of the layers above the substrate to form a gate stack 28. The photoresist mask is then removed to provide the structure shown in FIG. 4.

Referring now to FIG. 5, therein is shown the structure of FIG. 4 undergoing source/drain (S/D) extension junction implantation 30 to form S/D extension junctions 32 and 34 adjacent to the sides of the gate stack 28. The implantation 30 is a high-angle implantation to cause the dopant being implanted to be implanted under the GOX layer 20 as well as in the SOI layer 16.

Referring now to FIG. 6, therein is shown the structure of FIG. 5 having a barrier layer 38, generally an oxide layer, and a spacer layer 40, generally of an oxide or oxynitride deposited thereon. The barrier layer 38 tends to be much thinner than the spacer layer 40.

Referring now to FIG. 7, therein is shown the structure of FIG. 6 after an anisotropic etch to remove portions of the spacer layer 40 and a subsequent etch to remove portions of the barrier layer 38 to expose the SOI layer 16 and to form the sidewall spacer 44.

The sidewall spacer 44 is then used during an over-etch process of the SOI layer 16, which exposes the oxide layer 14 to form S/D contact trenches 46 and 48. The S/D contact trenches 46 and 48 are vertically inline with the sidewall spacer 44 on one side and have inwardly curved (as shown in FIG. 7 rather than linear) cross-sectional widths. The inwardly curved cross-section widths being defined as a number of successive widths taken horizontally from the top of a trench and progressing downwardly that are smaller than the one above in a smooth curve. The inward curve can progress to a point after which the inward curve blends into a vertical line where successive widths are no longer smaller than the one above. Each of the inwardly curved cross-sectional widths reduce in size from a top width "W" at the surface of the SOI layer 16 to below about 50% of the top width "W" at a sub-surface width "w" a distance "d" below the surface of the SOI layer 16. The sub-surface width "w" is preferably between about 50% and about 10% of the top width "W". The S/D contact trenches 46 and 48 can extend through the SOI layer 16 or stop short of the silicon oxide layer 14.

Referring now to FIG. 8, therein is shown the structure of FIG. 7 during a low-angle, four-quadrant implantation 50. The implantation 50 implants dopants that form S/D junctions 52 and 54 in the SOI layer 16.

Referring now to FIG. 9, therein is shown the structure of FIG. 8, after a rapid thermal anneal (RTA) which causes enhanced thermal diffusion (TED) of the S/D junctions 52 and 54 and the S/D extension junctions 32 and 34. The S/D junctions 52 and 54 extend vertically and the S/D extension junctions 32 and 34 extend horizontally.

The TED causes the closest point, or points of highest doping, of the S/D extension junctions 32 and 34 to be below the surface of the SOI layer 16 rather than just at the surface of the SOI layer 16 and under the GOX layer 20. This closest distance is called the "channel", designated channel "C", and is conventionally at the surface of the silicon just below the GOX layer 20. By having the channel "C" a depth "D" in the SOI layer 16, the capacitance effect caused by the overlap of the S/D extension junctions 32 and 34 under the GOX layer 20 and the polysilicon layer 22 are reduced. By reducing these parasitic capacitances, the performance of the semiconductor device 10 will be improved.

Also shown in FIG. 9 are optional salicided S/D contact areas 56 and 58 and a gate contact area 60. The salicided S/D contact areas 56 and 58 respectively line

the S/D contact trenches 46 and 48. The contact areas are generally vertical and are of such materials as tungsten silicide (WSi) or titanium silicide (TiSi) that form in the presence of silicon. Thus, the S/D regions of the SOI layer 16 are completely salicided.

Referring now to FIG. 10, therein is shown the structure of FIG 9 after the deposition, patterning, developing, and etching of a contact interlayer dielectric (ILD) 62 and a channel layer ILD 64. Also shown is the deposition of a conductive metal channel 68 and a conductive metal contact 70 to the salicided contact area 56 and of a channel 72 and its contact 74 to the salicided contact area 58. The channel 68 and its contact 70 can be deposited at one time as can the channel 72 and its contact 74, which can be metals such as aluminum (Al) and tungsten (W) The conductive metal contacts 70 and 74 have the same width down to the top surface of the SOI layer 16 and form vertical S/D contacts with the salicided contact areas 56 and 58 and fill the S/D contact trenches 46 and 48 (of FIG. 8).

The salicided contact areas 56 and 58 are shown exaggerated in size but are thin enough so that the conductive contacts 70 and 74 can be described as being substantially vertically inline with the sidewall spacer 44 on one side and having inwardly curved (as shown in FIG. 10 rather than linear), cross-sectional widths. Each of the inwardly curved cross-sectional widths reduce in size from a top width at the surface of the SOI layer 16 to below about 50% of the top width at a sub-surface width a distance below the surface of the SOI layer 16. The sub-surface width is preferably between about 50% and about 10% of the top width. The conductive contacts 70 and 74 can extend through the SOI layer 16 or stop short of the silicon oxide layer 14.

It will be noted that the structure of the present invention allows the conductive contacts 70 or 74 to be slightly misaligned with the S/D contact trenches 46 and 48. The conductive contact 70 is shown over the sidewall spacer 44. Essentially, because of the width of the S/D contact trenches 46 and 48 being smaller than the conductive contacts 70 and 74, the conductive contacts 70 and 74 are considered to be self-aligning.

Referring now to FIG. 11, therein is shown a top view of the structure of FIG. 10. A top view of the gate stack 28 is shown with the contacts 70 and 74 and the salicided contact areas 56 and 58 in the contact trenches 46 and 48. It should be noted that the contacts 70 and 74 are generally square in cross section and are not of

equal length to the salicided contact areas 56 and 58, respectively. This is because the saliciding provides a sufficiently low resistance surface that a large cross-sectional contact area is not required. It should also be noted that the contacts 70 and 74 are generally rectangular in cross section below the surface of the SOI layer 16.

Referring now to FIG. 12, therein is shown an alternate embodiment to the structure shown in FIG. 10. The same numbers are used to describe the same elements as in FIG. 10. In FIG. 12, the saliciding step is eliminated which means that contacts 70' and 74' will be in conductive contact directly with the SOI layer 16. Where there is direct contact between the contact metal and silicon, the conductivity will be reduced. Thus, the resistance between the contacts 70' and 74' and the SOI layer 16 is relatively large.

Referring now to FIG. 13, therein is shown a top view of the structure of FIG. 12. To increase the conductivity and reduce the resistance, 70' and 74' are made rectangular to cover as much of the S/D junctions 52 and 54, and the S/D extension junctions 32 and 34 as possible. Thus, the conductive metal contacts 70' and 74' make and form vertical S/D contacts.

While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations that fall within the spirit and scope of the included claims. All matters set forth herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

CLAIMS:

1. A semiconductor device [10] comprising:

a semiconductor substrate [16] having a contact trench [46] provided therein;

a gate [22] dielectric [20] disposed over the semiconductor substrate [16]adjacent the contact trench [46];

a gate [22] disposed over the gate dielectric [20];

a source/drain junction [52] disposed in the semiconductor substrate [16] adjacent the contact trench [46]; and

a conductive contact [70] disposed in the contact trench [46] conductively connected to the source/drain junction [52], the conductive contact [70] having inwardly curved cross-sectional widths in the semiconductor substrate [16].

2. The semiconductor device [10] as claimed in claim 1 wherein the conductive contact [70] has the inwardly curved cross-sectional widths with a top width and a sub-surface width in the semiconductor substrate [16], the sub-surface width is less than about 50% of the top width.

3. The semiconductor device [10] as claimed in claim 1 wherein the conductive contact [70] has the inwardly curved cross-sectional widths with a top width and a sub-surface width in the semiconductor substrate [16], the sub-surface width is between about 50% and about 10% of the top width.

4. The semiconductor device [10] as claimed in claim 1 wherein the source/drain junction [52] includes an extension source/drain junction [32] having a highest doping concentration below the surface of the semiconductor substrate [16].

5. The semiconductor device [10] as claimed in claim 1 including:

an insulator layer [14] disposed below the semiconductor substrate [16]; and

a further semiconductor substrate [12] disposed below the insulator layer [14].

6. A method of manufacturing a semiconductor device [10], comprising the steps of:

providing a semiconductor substrate [16];

forming a gate dielectric layer [20] over the semiconductor substrate [16];

forming a gate layer [22] over the gate dielectric layer [20];

etching the gate dielectric layer [20] and the gate layer [22] to form a gate stack [28];

implanting source/drain junctions [52] [54] adjacent the sides of the gate stack [28];

forming contact trenches [46] [48] in the semiconductor substrate [16] to expose the source/drain junctions [52] [54], the contact trenches [46] [48] adjacent the opposite

sides of the gate stack [28], the contact trenches [46] [48] having inwardly curved cross-sectional widths; and

forming conductive contacts [70] [72] in the contact trenches [46] [48] conductively connected with the source/drain junctions [52] [54], the conductive contacts [70] [72] having inwardly curved cross-sectional widths in the semiconductor substrate [16].

7. The method of manufacturing a semiconductor device [10] as claimed in claim 6 wherein the forming the conductive contacts [70] [72] forms the inwardly curved cross-sectional widths with top widths and sub-surface widths in the semiconductor substrate [16], the sub-surface widths are less than about 50% of the widths of the top widths.

8. The method of manufacturing a semiconductor device [10] as claimed in claim 6 wherein the step of forming the conductive contacts [70] [72] forms the inwardly curved cross-sectional widths with top width and sub-surface widths in the semiconductor substrate [16], the sub-surface widths are between about 50% and about 10% of the widths of the top widths.

9. The method of manufacturing a semiconductor device [10] as claimed in claim 6 wherein the forming the source/drain junctions [52] [54] include forming extension source/drain junctions [32] [34] in the semiconductor substrate [16] and forming the extension source/drain junctions [32] [34] closest together below the surface of the semiconductor substrate [16].

10. The method of manufacturing a semiconductor device [10] as claimed in claim 6 including:

providing a further semiconductor substrate [12]; and

forming an insulator layer [14] on the further semiconductor substrate [12] for the semiconductor substrate [16] to be formed on to form a semiconductor on insulator structure.