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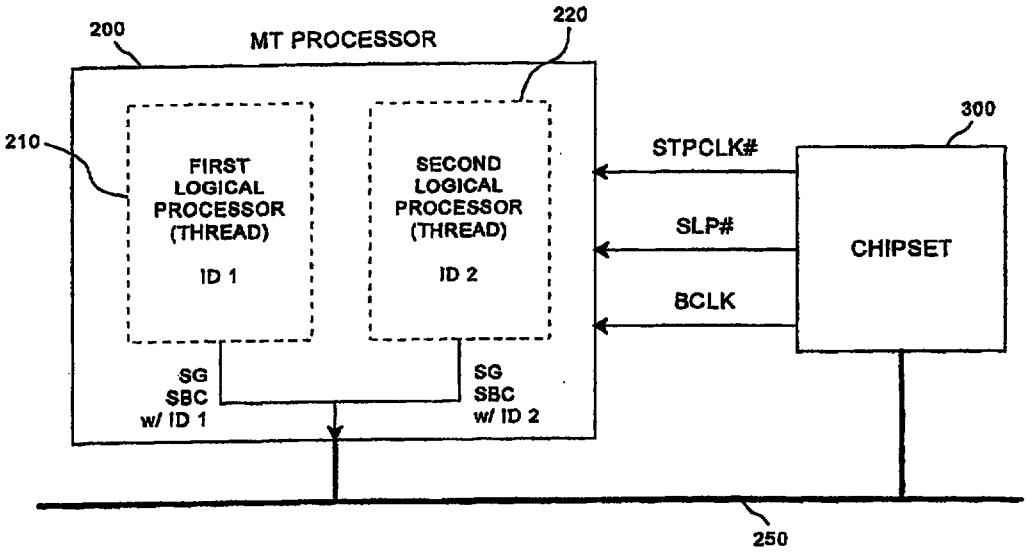
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(54) Title: METHOD AND APPARATUS FOR POWER MODE TRANSITION IN A MULTI-THREAD PROCESSOR



(57) Abstract

A method and apparatus for power mode transition in a multi-thread processor (200). A first indication is issued, including a first identifier associated with a first logical processor (210) in a processor, that the first logical processor has entered a power mode. A second indication is issued, including a second identifier associated with a second logical processor (220) in the processor, that the second logical processor has entered the power mode. The indications may be, for example, stop grant acknowledge special bus cycles indicating that the logical processors have entered a stop grant mode. The processor may be transitioned to a sleep mode when both the first and second indications have been issued.