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PATENT SPECIFICATION

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COMPLETE SPECIFICATION

Semiconductor Circuits

We, TEXAS INSTRUMENTS INCORPORATED, of 13500 North Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement: —

This invention relates to semiconductor devices and methods of making same, and more particularly to semiconductor devices including two circuit elements which are different in kind from one another.

Many methods and techniques for miniaturizing electronic circuits have been proposed in the past. At first, most of the effort was spent upon reducing the size of the components and packing them more closely together. Work directed toward reducing component size is still going on, but has nearly reached a limit. Other efforts have been made to reduce the size of electronic circuits, such as by eliminating the protective coverings from components, by using more or less conventional techniques to form the components of a complete circuit on a single substrate, and by providing the components with a uniform size and shape to permit closer spacings in the circuit packaging therefor.

All of these methods and techniques require a very large number and variety of operations in fabricating a complete circuit. For example, of all circuit components, resistors are usually considered the most simple to form, but when adapted for miniaturization by conventional techniques, fabrication requires at least the following steps:

a. Formation of the substrate
b. Preparation of the substrate
c. Application of terminations
d. Preparation of resistor material
e. Application of the resistor material
f. Heat treatment of the resistor material
g. Protection or stabilization of the resistor

Capacitors, transistors, and diodes, when adapted for miniaturization, each require at least as many steps in the fabrication thereof. Unfortunately, many of the steps required are not compatible. A treatment that is desirable for the protection of a resistor may damage another element formed on the same substrate, such as a capacitor or transistor, and as the size of the complete circuit is reduced, such conflicting treatments, or interactions, become of increasing importance. Interactions may be minimized by forming the components separately and then assembling them into a complete package, but the very act of assembly may cause damage to the more sensitive components.

Because of the large number of operations required, control over miniaturized circuit fabrication becomes very difficult. To illustrate, many raw materials must be evaluated and controlled, even though they may not be well understood. Further, many testing operations are required and, even though a high yield may be obtained for each operation, so many operations are required that the over-all yield is often quite low. In service, the reliability of a circuit produced by methods of such complexity may also be quite low due to the tremendous number of controls required. Additionally, the separate formation of individual components requires individual terminations for each component. These terminations may eventually become as small as a dot of conductive paint. However, they still account for a large fraction of the usable area or volume of the circuit, and may become an additional cause of cir-

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cuit failure or rejection due to misalignment.

In contrast to the approaches to miniaturization that have been made in the past, the present invention has resulted from a new and totally different concept for miniaturization. Semiconductor circuits or devices made in accordance with this concept are the subject matter of our co-pending patent application No. 3633/60 (Serial No. 945,734).

The present invention is a semiconductor circuit comprising a wafer of single crystal semiconductor material having a plurality of first regions each having a conductivity type opposite to that of the region immediately underlying such first region thereby to form a plurality of corresponding P-N junctions extending to one major wafer face and there defining a corresponding plurality of enclosed areas each occupying a limited portion of the area of said one major face and spaced from one another on said one major face, said wafer having an elongated portion thereof providing a current path generally parallel to said one major face, said elongated portion having one end thereof connected to a bias potential and the other end thereof ohmically connected to said regions immediately underlying said first regions for applying substantially the same potential thereto, and input connections respectively to said first regions for receiving input signals.

In a specific embodiment of the invention, components or circuit elements of a bistable multivibrator circuit are formed in or near one surface of a relatively thin semiconductor wafer, strip or layer which is in or on one surface of a semiconductor substrate.

Circuit elements in the semiconductor wafer may be effectively electrically isolated through the advantageous employment of electrical and/or mechanical shaping as described in detail in said co-pending patent application No. 3633/60 (Serial No. 945,734). As a result, the final circuit is arranged in essentially planar form.

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:—

Fig. 1 illustrates a top plan view of a semiconductor device embodying the invention;

Fig. 2A illustrates a schematic circuit diagram of the semiconductor device illustrated in Fig. 1;

Figs. 2B and 2C illustrate circuit diagrams showing variations in the circuit illustrated in Figs. 1 and 2A; and

Figs. 3 to 6, inclusive, show cross sectional views of some of the semiconductor circuit elements illustrated in Fig. 1.

With reference to the drawings, embodiments of the invention will now be described in detail in order to provide a better understanding of the principles of the invention and the various forms and embodiments thereof.

One embodiment of the invention is a semiconductor device including the circuit elements of a bistable multivibrator utilizing a diode gate and a reversed biased diode for biasing said gate. The semiconductor device comprises a body of semiconductor material of single crystal structure, and can be composed of any suitable semiconductor material such as germanium, silicon, intermetallic alloys such as gallium arsenide, aluminium antimonide, indium antimonide, as well as others.

With reference to Fig. 1, there is shown a semiconductor device which provides the gated bistable multivibrator operation. Strips or layers 12 and 14 of single crystal semiconductor material are illustrated as being mounted or secured on substrate 10, for example, by solder glass. Intrinsic semiconductor material has a relatively high order of resistivity and the substrate 10 may be formed therefrom. The substrate 10 may be either a separate block of intrinsic material on which layers 12 and 14 are secured, or it may be part of the same physical piece of semiconductor material as layers 12 and 14. According to the latter, the entire unit is formed from a block of intrinsic semiconductor material into which doping impurities are diffused in the regions occupied by the layers 12 and 14 which layers differ from the substrate in their electrical characteristics due to the impurity doping. The space 16 between the two layers may be formed by originally starting with a single large layer of semiconductor material and etching to divide the large layer into two portions or layers. However, the purpose of this shaping operation is to provide isolation between the circuit elements integrated with or in layers 12 and 14, and it is to be understood that substantial electrical isolation may be obtained by means other than etching completely through a larger layer to form two layers; for example, electrical isolation could be provided by a high resistance area in the semiconductor material between circuit elements desired to be isolated. This high resistance provides a substantial open circuit to prevent undesired interference between the circuit elements involved. However, in the embodiment illustrated in Fig. 1, isolation between the two layers is provided by etching the space 16 in an original large layer to form two layers 12 and 14 which are physically separated, one from the other.

As described in said co-pending patent application No. 3633/60 (Serial No. 945,734), the original crystal may have firstly formed therein by diffusion a layer of P-type semiconductor material to form a P-N junction. Circuit components may then be formed

therein by selective etching of the semiconductor material and by selectively diffusing N-type material into the P layer. Metal contacts may then be plated or evaporated onto desired layers to form electrical connections.

Formed in layer 12 is transistor TR-2 of the NPN type with a second N region diffused in the P-type base to form in effect a two-emitter transistor. A cross sectional view of TR-2 is shown in Figure 3, and this transistor is the subject matter of our copending patent application No. 46086/63 (Serial No. 958,245). This double emitter structure actually provides one NPN transistor plus an integral diode formed by the additional diffused PN junction. TR-2 has an N-type collector region 18 provided by the layer 12, a P-type base region 20 and two N-type emitter regions 22 and 24. Ohmic contacts 26, 28 and 30 are plated or evaporated onto their corresponding semiconductor layers. Output lead 33 is soldered or alloyed to substrate 10, and extends beneath the left-hand end of layer 12 and makes ohmic contact therewith, and thereby also with collector region 18 of TR-2. Double emitter transistor TR-3 is identical with TR-2.

Contiguous with base region 20 is a strip or elongated portion 32 of P-type material formed by diffusion into layer 12 and formed in a tortuous path to define a cross-coupling resistor R_1 having a value of 7 kilohms (K). The left-half 34 of layer 12, a portion of which underlies P-strip 32, defines a bias resistor R_2 having a value of 5K. An ohmic contact 36 is formed on the other end of P-strip 32 to provide means for electrically connecting this end of R_1 to the output lead 38. Resistance R_2 is connected to the bias lead 40 which is mounted on substrate 10 and passes beneath layer 12 into ohmic contact therewith. P-strip or elongated portion 42 and its corresponding underlying end crystal portion 44 define resistors R_3 and R_4 in an identical manner. The distributed capacitance at the PN junctions formed by P-strips 32 and 42, with their underlying corresponding N-strip portions provide a distributed capacitance equivalent to capacitors C_3 and C_4, each having a value of 1000 micromicrofarads.

Also formed in N-layer 12 is the transistor TR-1 having a collector region defined by an area of layer 12, a diffused P-layer 45 (Figure 1) defining a base region and a diffused N-layer 46 defining an emitter region. An ohmic contact 48 is plated on the emitter layer 46 and an ohmic contact 50 is plated on the base layer 45 so that electrical leads may be interconnected between these contacts and other elements, as described below. In cross section, TR-1 is similar to Figure 3 with the exception that TR-1 has only one diffused emitter region instead of two. Even though TR-1 has the form of a transistor, it provides two junction diodes by means of its collector-base and emitter-base PN junctions. In this embodiment of the invention, the structure is utilized as two separate PN junction diodes D_1 and D_4 rather than to provide conventional transistor action.

Also formed in layer 12 is a PN junction diode D_3, a cross sectional view of which is shown in Figure 6. This diode is formed of a PN junction comprising a region 52 of the N-crystal and a P-region 54 formed therein by diffusion and carrying an ohmic contact 56.

A P-layer or region 58 formed in N-layer 14 by diffusion is not etched away, and two N-layers or regions are formed in P-layer 58 by diffusion to form identical junction diodes D_2 and D_7. A cross sectional view of diode D_2 is shown in Figure 4. In this case, the PN junction is formed between the P-layer 58 and the N-layer 60 with the N-strip 14 merely acting as a substrate. A metal contact 62 is plated on N-layer 60 to provide means for interconnecting the junction with other circuit components or leads.

Also formed on layer 14 are two oxide-type semiconductor network coupling capacitors C_1 and C_2 formed as described in our copending patent application No. 5691/62 (Serial No. 945,737). As shown in Figure 5, oxide capacitor C_1 comprises a silicon dioxide coating 64 on P-layer 58. This coating acts as a dielectric for the capacitor C_1. A metal plate 66 is then plated on top of oxide coating 64 to complete formation of the capacitor. The capacitor is defined by the two conductors, P-layer 58 and metal plate 66, separated by the dielectric oxide coating 64.

Additional leads are attached to the substrate 10, and are utilized when this bistable multivibrator is connected as a part of a binary counter. These leads are as follows: input lead 68; clear lead 70; set lead 72; lockout lead 74; ground lead 76. External wires, as shown in Figure 1, interconnect the various circuit components with each other, and with the leads in a manner to provide bistable multivibrator operation.

The general operation of the semiconductor network illustrated in Figure 1 and just described will be briefly described to provide a better understanding of the structure of the semiconductor network device of Figure 1. Figures 2*b* and 2*c* provide the same operation as Figure 2*a*, but differ in circuit design. Semiconductor networks could also be constructed to conform exactly with the circuits shown in Figures 2*b* and 2*c*. For example, the difference between Figures 2*a* and 2*b* involves diodes D_1, D_4, D_5 and D_6. These diodes are shown as separate circuit elements in Figure 2*b*, but are incorporated

in other structures in Figure 2*a*. In Figure 2*a*, the diodes D_1 and D_4 are defined by the emitter-base and base-collector junction diodes respectively of TR-1, and diodes D_5 and D_6 of Figure 2*b* are incorporated in transistors TR-2 and TR-3 of Figure 2*a* in the form of second emitter base junctions.

Another difference between Figures 2*a* and 2*b* is that the cross-coupling capacitors C_3 and C_4 of Figure 2*b* have been replaced by the distributed capacitance between their corresponding semiconductor network 5K and 7K resistors R_1 and R_2, and R_3 and R_4. As described above with respect to the semiconductor network of Figure 2*a*, R_1 and R_3 are formed by P-strips 32 and 42, respectively, and R_2 and R_4 are formed by N-crystal portions 34 and 44, respectively. Since the polarity across the capacitance thus formed is always the same, the junction-type distributed capacitance satisfactory.

The difference between Figures 2*b* and 2*c* is that the 100 K. resistors R_{11}, R_{8}, R_7 and R_9 of Figure 2*c* are replaced by reverse biased PN junction diodes D_1, D_2, D_3 and D_4, respectively, of Figure 2*b*. The purpose of these 100 K. resistors, shown in Figure 2*c*, is to supply current to reverse bias the diode gates D_5, D_6 and D_7. Although this multivibrator circuit could be constructed as a miniature semiconductor network to correspond exactly with the schematic illustrated in Figure 2*c*, semiconductor network techniques do not lend themselves as easily to providing high valued resistances such as the 100 K. resistors R_5—R_8, inclusive. In particular, 100 K, resistors require either very high resistivity semiconductor material or a large amount of space for a long path in lower resistivity material. Since the purpose of these resistors is to supply current to back bias diode gates, this current may also be obtained by replacing the resistors with reverse biased PN junction diodes, effectively placing the diode gate and the biasing diode in series. Such substitutions result in the differences between the diagram shown in Figures 2*b* and 2*c*, the circuit shown in Figure 2*b* being much easier to construct by semiconductor network techniques. These substitutions have been checked by temperature cycling the semiconductor network multivibrator and both the basic circuit of Figure 2*c* and the revised circuit of Figure 2*b* operate properly up to 110° C.

The gated bistable multivibrator shown in Figure 2*a* is designed for use as one stage of a binary counter. The set input lead is utilized to determine which transistor will be initially conducting and which initially non-conducting. Since both TR-2 and TR-3 are NPN transistors, a positive pulse on the base of transistor TR-2 will render that transistor conducting and TR-3 non-conducting. Negative trigger pulses may then be applied to the input lead through diode D_7, coupling capacitor C_1 and diode D_5 to cut off transistor TR-2 and render transistor TR-3 conducting. A second trigger pulse will return the circuit to its original condition. Selective application of pulses to the lockout lead may lock out or block trigger pulses applied to the input lead to render the multivibrator circuit insensitive to input pulses. A positive polarity pulse applied to the clear lead will return the circuit to its original condition. Output 1 and output 2 supply pulses indicative of the state of their corresponding transistor.

Therefore, Figure 2*a* illustrates a basic gated bistable multivibrator circuit diagram which represents the operation of the semiconductor network of Figure 1. Figure 2*b* is the equivalent of Figure 2*c*, and also represents exactly the operation of Figure 1. However, in Figure 2*b*, the 100 K. resistors 2*c* have been replaced by reverse biased PN junction diodes. Figure 2*a* again is the full equivalent as far as operation is concerned of Figures 2*b* and 2*c*, but in order to adapt the circuit more easily to semiconductor solid network techniques, two separate diodes have been combined into a single transistor structure as collector base and emitter base diodes. In addition, two other diodes have been replaced by an additional emitter-base junction in each of the switching transistors TR-2 and TR-3.

Reference is additionally made to our co-pending parent patent application No. 16071/60 (Serial No. 958242) from which the present application is divided, and to our co-pending patent applications Nos. 23279/63; 46087/63; 46088/63 and 46089/63 (Serial Nos. 958244; 958246; 958247 and 958248), also divided from said parent patent application.

Terms indicative of position, such as "on" and "overlying", are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor device could be used in any desired positional orientation.

It must be emphasized here that only several preferred embodiments of this invention have been described above, and that other variations and modifications thereof may be made without departing from the scope of this invention, which is defined in the appended claims.

WHAT WE CLAIM IS:—

1. A semiconductor circuit comprising a wafer of single crystal semiconductor material having a plurality of first regions each having a conductivity type opposite to that of the region immediately underlying such first region thereby to form a plurality of corresponding P—N junctions extending to one major wafer face and there defining a corres-

in other structures in Figure 2*a*. In Figure 2*a*, the diodes D_1 and D_4 are defined by the emitter-base and base-collector junction diodes respectively of TR-1, and diodes D_5 and D_6 of Figure 2*b* are incorporated in transistors TR-2 and TR-3 of Figure 2*a* in the form of second emitter base junctions.

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ponding plurality of enclosed areas each occupying a limited portion of the area of said one major face and spaced from one another on said one major face, said wafer having an elongated portion thereof providing a current path generally parallel to said one major face, said elongated portion having one end thereof connected to a bias potential and the other end thereof ohmically connected to said regions immediately underlying said first regions for applying substantially the same potential thereto, and input connections respectively to said first regions for receiving input signals.

2. A semiconductor circuit according to claim 1, including a corresponding plurality of second regions overlying and contiguous with respective ones of said first regions to form with said first regions a corresponding plurality of P—N junctions.

3. A semiconductor circuit according to either preceding claim, wherein said wafer has a further region having a conductivity type opposite to that of the region immediately underlying it thereby to form a further P—N junction extending to said one major face and there defining a further enclosed area occupying a limited portion of the area of said one major face and being spaced from the other enclosed areas on said one major face, and said further region being ohmically connected to said regions immediately underlying said first regions.

4. A semiconductor circuit according to claim 3, including a third region overlying and contiguous with said further region to form a P—N junction and an output connection to said region immediately underlying said further region.

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