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(54) Title: INTEGRATED CIRCUIT WITH TUNABLE CAPACITOR ARRAY

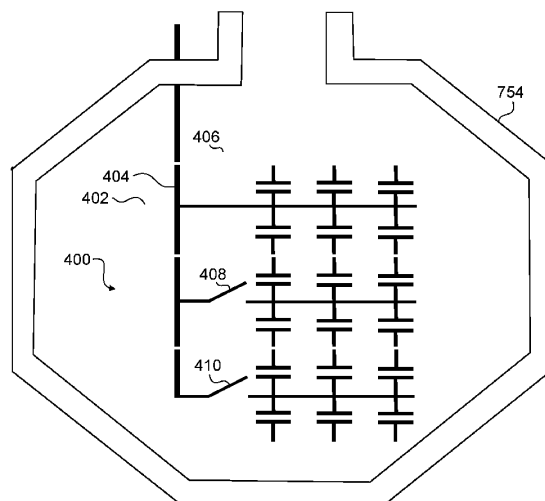


FIG. 9

(57) Abstract: The present disclosure describes a semiconductor structure that is resistant to induced eddy currents. The semiconductor device includes a substrate, a device layer having electronic devices on the substrate, and a metallization layer above the device layer. The first metallization layer includes first and second terminal traces, a switch, and capacitors. A first terminal of a capacitor of the capacitors is coupled to the first terminal trace via the switch. A second terminal of the capacitor is coupled to the second terminal trace. The first and second terminal traces are disposed along the same side of the capacitors.

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