A NEW METHOD TO PREVENT SIDE DAMAGE OF METAL DURING VIA ETCH

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to a method of metallization in the fabrication of integrated circuits, and more particularly, to a method of preventing via failures due to misalignment during metallization in the fabrication of integrated circuits.

(2) Description of the Prior Art

As the misalignment margin for lithography processes decreases with device scaling, misalignment becomes a key issue in integrated circuit processes. A misaligned via hole to a metal line may lead to via failure. Fluorine used during tungsten chemical vapor deposition (CVD) may attack the metal line exposed by the via opening's misalignment and form aluminum fluoride, an insulator. This will cause via failure. It is desired to prevent attack of the metal line in the case of via opening misalignment.

U.S. Patent 5,756,396 to Lee et al teaches forming titanium nitride and tungsten spacers on the sidewalls of metal lines. U.S. Patents 5,858,875, 5,757,077,

and 5,656,543 to Chung et al all disclose silicon nitride etch stop spacers on the sidewalls of metal lines. U.S. Patent 5,617,072 to Mehta discloses insulating spacers on the sidewalls of metal lines. The thick insulating spacers may cause a gap fill problem and may not protect the metal as well during etching as would a conducting spacer.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of via metallization in the fabrication of an integrated circuit.

Another object of the present invention is to provide an effective and very manufacturable method of preventing via failure caused by via misalignment to a metal line in the fabrication of an integrated circuit.

Another object of the present invention is to provide a method for preventing via failure caused by misalignment to a metal line by forming conductive spacers on the metal line.

A further object of the invention is to provide conductive spacers on a metal line to prevent side

damage to the metal during via etching in the fabrication of integrated circuits.

In accordance with the objects of this invention a new method of preventing via failure caused by misalignment to a metal line by forming conductive spacers on the metal line is achieved. Semiconductor device structures in and on a semiconductor substrate and covered with an insulating layer. Metal lines are formed overlying the insulating layer. Conductive spacers of titanium or titanium nitride are formed on the sidewalls of said metal lines. An intermetal dielectric layer is deposited over the metal lines. Via openings are etched through the intermetal dielectric layer to the metal lines wherein there is a misalignment of the via openings to the metal lines and wherein an edge of the metal lines is exposed by the misalignment. A barrier layer is deposited within the via openings and does not cover the exposed edge of the metal lines. A tungsten layer is deposited within the via openings using WF_6 gas to form metal plugs. The conductive spacers protect the exposed edge of the metal lines thereby preventing attack of the metal lines by fluorine ions. This completes fabrication of the integrated circuit without via failure.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Fig. 1 schematically illustrates in cross-sectional representation a via failure of the prior art.

Figs. 2 through 9 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 illustrates an example of the via failure problem of the prior art. Metal lines 20 have been formed over the semiconductor substrate 10 and covered with intermetal dielectric (IMD) layer 30. Via openings 35 have been etched through the IMD layer 30 to the underlying metal lines. Misalignment of the etching mask causes the IMD to be overetched, for example, at the left side of the metal line, as shown in the figure. A portion 37 of the metal line is damaged. A narrow contact hole 39 is generated at the edge of the metal line.

Next, a barrier metal layer is deposited over the IMD layer and within the via openings. Step coverage of the barrier metal layer 40 is poor at the narrow contact. When tungsten is deposited by CVD using WF_6 gas, the fluorine will attack the exposed aluminum not covered by the barrier layer in the area of 39 and will form aluminum fluoride, an insulator. This will cause via failure.

The present invention prevents via failure by forming a conductive spacer on the sidewalls of the metal line.

Referring now more particularly to Fig. 2, there is illustrated a portion of a partially completed integrated circuit. There is shown a semiconductor substrate 10, preferably composed of monocrystalline silicon. Isolation, such as field oxide regions or shallow trench isolation, not shown, are formed as is conventional in the art in the semiconductor substrate 10. Semiconductor device structures, including gate electrode and source and drain regions, not shown, may be fabricated in and on the semiconductor substrate. A thick insulating layer of silicon dioxide or borophosphosilicate glass (BPSG), or the like, is blanket deposited over the semiconductor device structures. All of these layers and devices are represented in the

figures by substrate layer 10.

Metal lines are now fabricated over the substrate. These lines may contact some of the device structures within the substrate, such as through a tungsten plug, not shown. A barrier layer 18 is deposited over the substrate. This may be titanium nitride or titanium/titanium nitride having a thickness of between about 100 and 1000 Angstroms.

The metal layer 20 is deposited over the barrier layer 18. The metal layer comprises Aluminum or an Aluminum alloy such as AlSi, AlCu, or AlSiCu and is sputter deposited to a thickness of between about 3000 and 10,000 Angstroms. An anti-reflective coating (ARC) 22, such as titanium or titanium/titanium nitride, may be deposited over the metal layer 20. The metal line stack is patterned as shown to form the metal lines 20.

Now, the blocking layer of the present invention is to be deposited as shown in Fig. 3. A layer of titanium or titanium nitride 24 is deposited conformally by physical vapor deposition, chemical vapor deposition, or the like, over the patterned metal lines to a thickness of between about 100 and 1000 Angstroms. The blocking layer of

the present invention comprises a conducting material. This increases via etch resistance, blocks phosphorus penetration, and prevents chemical reaction with the aluminum. Additionally, the gap-fill quality is better with the conductive film than it would be with an insulating film in a very narrow metal line spacing because a similar material (both conducting) will deposit better into the gap.

Referring now to Fig. 4, the blocking layer 24 is anisotropically etched away to leave conducting spacers 26 on the sidewalls of the metal lines. The titanium or titanium nitride spacers 26 have a thickness of between about 100 and 1000 Angstroms. This smaller thickness than the thickness of the double spacers of the prior art improves gap fill capability of the subsequent intermetal dielectric layer.

Now, an intermetal dielectric (IMD) layer 30 is deposited over the metal lines and filling the gap between the metal lines, and then planarized, such as by chemical mechanical polishing (CMP), as shown in Fig. 5. The IMD layer may comprise a single layer or a multi-layer of silicon dioxide, tetraethoxysilane (TEOS) oxide, borophosphosilicate glass (BPSG), or the like and have a post-CMP thickness of between about 5000 and 20,000 Angstroms.

Referring now to Fig. 6, the via mask is applied. Photoresist mask 35 is shown over the IMD layer 30. The mask has been misaligned slightly 31 to the left. Now, the via openings 39 are etched, as shown in Fig. 7. The etch resistance of the conductive spacer 26 is much higher than would be the etch resistance of an insulator spacer. The conductive spacers 26 protect the metal line 20 from damage during etching even with mask misalignment, as shown in the example.

Now, the barrier layer 40 is deposited over the IMD layer and within the via openings, as shown in Fig. 8. The barrier layer may be titanium or titanium nitride or a combination of the two and have a thickness of between about 100 and 1000 Angstroms. As before, the barrier layer 40 has poor step coverage within the narrow portion of the via opening at the edge of the metal line. However, the conductive spacer 26 covers the portion of the metal line exposed by the misalignment of the via etch.

Tungsten is deposited by CVD as is conventional. There is no attack of the metal line by the fluorine in the WF_6 precursor because the conductive spacer protects the metal line. Completed tungsten plugs 44 are shown in Fig. 9.

Processing is completed as is conventional, with further metallization, as required by the design of the integrated circuit device.

The process of the invention provides a simple method for preventing via failure. A thin spacer is formed on the sidewalls of the metal lines. The spacer material is a conductive material that will not be etched away during the via etch. The spacers protect the metal sidewall exposed by misaligned via etching from attack by fluorine, thereby preventing via failure.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.



CLAIMS

1. A method of metallization in the fabrication of an integrated circuit comprising:

providing semiconductor device structures in and on a semiconductor substrate;

covering said semiconductor device structures with an insulating layer;

forming metal lines overlying said insulating layer;

forming conductive spacers on the sidewalls of said metal lines;

depositing an intermetal dielectric layer over said metal lines;

etching via openings through said intermetal dielectric layer to said metal lines;

depositing a barrier layer within said via openings; and

depositing a metal layer overlying said barrier layer and within said via openings to form metal plugs completing said fabrication of said integrated circuit.

2. The method according to Claim 1 wherein said semiconductor device structures include gate electrodes and source and drain regions.



3. The method according to Claim 1 wherein said metal lines comprise:

a barrier metal layer overlying said insulating layer;

an aluminum layer overlying said barrier layer; and

an anti-reflective coating layer overlying said aluminum layer.

4. The method according to Claim 3 wherein said barrier metal layer comprises titanium having a thickness of between about 100 and 500 Angstroms.

5. The method according to Claim 3 wherein said barrier metal layer comprises titanium nitride having a thickness of between about 100 and 500 Angstroms.

6. The method according to Claim 1 wherein said metal lines comprise one of the group containing aluminum and aluminum alloys having a thickness of between about 4000 and 8000 Angstroms.

7. The method according to Claim 1 wherein said conductive spacers comprise titanium and have a thickness of between about 100 and 1000 Angstroms.



8. The method according to Claim 1 wherein said conductive spacers comprise titanium nitride and have a thickness of between about 100 and 1000 Angstroms.

9. The method according to Claim 1 wherein there is a misalignment of said via openings to said metal lines and wherein said conductive spacers protect an edge of said metal line exposed by said misalignment of said via openings to prevent via failure.

10. The method according to Claim 1 wherein said barrier layer comprises titanium/titanium nitride having a thickness of between about 100 and 1000 Angstroms.

11. The method according to Claim 1 wherein said metal layer comprises tungsten deposited by chemical vapor deposition using WF_6 gas.

12. A method of metallization in the fabrication of an integrated circuit comprising:

providing semiconductor device structures in and on a semiconductor substrate;

covering said semiconductor device structures with an insulating layer;

forming metal lines overlying said insulating



layer;

forming conductive spacers on the sidewalls of said metal lines;

depositing an intermetal dielectric layer over said metal lines;

etching via openings through said intermetal dielectric layer to said metal lines wherein there is a misalignment of said via openings to said metal lines and wherein an edge of said metal lines is exposed by said misalignment of said via openings;

depositing a barrier layer within said via openings wherein said barrier layer does not cover said edge of said metal lines exposed by said misalignment of said via openings; and

depositing a metal layer overlying said barrier layer and within said via openings to form metal plugs wherein said conductive spacers protect said edge of said metal lines exposed by said misalignment of said via openings and thereby prevent attack of said metal lines by ions used in said step of depositing said metal layer completing said fabrication of said integrated circuit.

13. The method according to Claim 12 wherein said semiconductor device structures include gate electrodes



and source and drain regions.

14. The method according to Claim 12 wherein said metal lines comprise:

a barrier metal layer overlying said insulating layer;

an aluminum layer overlying said barrier layer; and

an anti-reflective coating layer overlying said aluminum layer.

15. The method according to Claim 14 wherein said barrier metal layer comprises titanium having a thickness of between about 100 and 500 Angstroms.

16. The method according to Claim 14 wherein said barrier metal layer comprises titanium nitride having a thickness of between about 100 and 500 Angstroms.

17. The method according to Claim 12 wherein said metal lines comprise one of the group containing aluminum and aluminum alloys having a thickness of between about 4000 and 8000 Angstroms.

18. The method according to Claim 12 wherein said conductive spacers comprise titanium and have a



thickness of between about 100 and 1000 Angstroms.

19. The method according to Claim 12 wherein said conductive spacers comprise titanium nitride and have a thickness of between about 100 and 1000 Angstroms.

20. The method according to Claim 12 wherein said barrier layer comprises titanium/titanium nitride having a thickness of between about 100 and 500 Angstroms.

21. The method according to Claim 12 wherein said metal layer comprises tungsten deposited by chemical vapor deposition using WF_6 gas.

22. A method of metallization in the fabrication of an integrated circuit comprising:

providing semiconductor device structures in and on a semiconductor substrate;

covering said semiconductor device structures with an insulating layer;

forming aluminum lines overlying said insulating layer;

forming conductive spacers on the sidewalls of said aluminum lines wherein said conductive spacers comprise one of the group containing titanium and

titanium nitride;

depositing an intermetal dielectric layer over said aluminum lines;

etching via openings through said intermetal dielectric layer to said aluminum lines wherein there is a misalignment of said via openings to said aluminum lines and wherein an edge of said aluminum lines is exposed by said misalignment of said via openings;

depositing a barrier layer within said via openings wherein said barrier layer does not cover said edge of said aluminum lines exposed by said misalignment of said via openings; and

depositing a tungsten layer using WF_6 gas overlying said barrier layer and within said via openings to form metal plugs wherein said conductive spacers protect said edge of said aluminum lines exposed by said misalignment of said via openings and thereby prevent attack of said aluminum lines by fluorine ions used in said step of depositing said tungsten layer completing said fabrication of said integrated circuit.

23. The method according to Claim 22 wherein said semiconductor device structures include gate electrodes and source and drain regions.



24. The method according to Claim 22 wherein said aluminum lines further comprise:

a barrier metal layer underlying said aluminum lines; and

an anti-reflective coating layer overlying said aluminum lines.

25. The method according to Claim 24 wherein said barrier layer comprises titanium having a thickness of between about 100 and 1000 Angstroms.

26. The method according to Claim 24 wherein said barrier layer comprises titanium nitride having a thickness of between about 100 and 1000 Angstroms.

27. The method according to Claim 22 wherein said conductive spacers have a thickness of between about 100 and 1000 Angstroms.

28. The method according to Claim 22 wherein said barrier layer comprises titanium/titanium nitride having a thickness of between about 100 and 500 Angstroms.