What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a trench extending in a first direction and dividing the semiconductor substrate into active areas adjacent to each other in a second direction intersecting the first direction;

~~a memory cell provided with a~~ control gate electrodes extending in the second direction~~on a charge storage layer via an interelectrode insulating film~~;

a select gate electrode extending in the second direction and adjacent to one of the control gate electrodes;~~and~~

~~a gap provided between the adjacent~~ charge storage layers arranged between the control gate electrodes and the semiconductor substrate~~in a word line direction and formed continuously over the adjacent memory cells in a bit line direction in a manner of sinking below the word line~~;

a select transistor including the select gate electrode and connected between one of memory cells and bit lines;

a gap formed in the trench to extend in the first direction, arranged between the adjacent charge storage layers in the second direction, and extending under the select gate electrode; and

a buried insulating film provided in the trench under the select gate electrode to be adjacent to the gap extending under the select gate electrode.

~~2. The nonvolatile semiconductor memory device according to claim 1, wherein the gap is formed along a trench isolating an active area of the memory cell.~~

~~3. The nonvolatile semiconductor memory device according to claim 2, wherein the gap enters the trench that isolates the active area of the memory cell and is provided in a semiconductor substrate.~~

~~4. The nonvolatile semiconductor memory device according to claim 3, wherein the gap is formed continuously in the trench over the adjacent memory cells in the bit line direction.~~

~~5. The nonvolatile semiconductor memory device according to claim 1, further comprising a space formed on the gap between the word lines.~~

~~6. The nonvolatile semiconductor memory device according to claim 1, further comprising a cover insulating film stretching over between the control gate electrodes in a manner.~~

~~7. The nonvolatile semiconductor memory device according to claim 1, wherein the gap is arranged in a manner where the interelectrode insulating film covers side walls of the charge storage layer.~~

2~~8~~. The nonvolatile semiconductor memory device according

to claim 1~~2~~, wherein assuming a gate length of the control gate electrode is L, and a height on the trench from an undersurface of the interelectrode insulating film to a top surface of the interelectrode insulating film on the charge storage layer is X, a depth D of the gap of when viewed from the top surface of the interelectrode insulating film on the trench satisfies a condition of $X + L/2 \leq D < 2X + L$.

3~~9~~. The nonvolatile semiconductor memory device according to claim 1 or 2, wherein the gap reaches to a position deeper than an undersurface of the charge storage layer.

~~10. The nonvolatile semiconductor memory device according to claim 1, further comprising a select gate electrode connecting an active area of the memory cell to the bit line, wherein the gap is separated below the select gate electrode.~~

4~~11~~. The nonvolatile semiconductor memory device according to any one of claims 1 to 3, further comprising:

a word line drawing part in which the word line drawn out from the memory cell is arranged;

and a buried insulating film buried the trench, wherein the buried insulating film is in contact with the interelectrode insulating film on the trench isolating the active area of the word line drawing part.

5~~12~~. The nonvolatile semiconductor memory device according

to any one of claims 1 to 4, further comprising:

a bit contact part in which a bit contact is formed; and

a reburied insulating film reburying the gap formed in a trench isolating an active area of the bit contact part.

~~13. The nonvolatile semiconductor memory device according to claim 2, wherein the interelectrode insulating film is formed continuously over the adjacent memory cells in the word line direction in a manner of stretching over the gap.~~

~~14. The nonvolatile semiconductor memory device according to claim 13, wherein the interelectrode insulating film is arranged in a position lower than a top of the charge storage layer on the gap.~~

6~~15~~. A method for manufacturing a nonvolatile semiconductor memory device, comprising:

depositing a floating gate electrode material on a semiconductor substrate via a tunnel insulating film;

forming a trench in the semiconductor substrate in a bit line direction via the floating gate electrode material and the tunnel insulating film;

forming a buried insulating film in the trench;

forming an interelectrode insulating film on the buried insulating film and the floating gate electrode material;

depositing a control gate electrode material on the interelectrode insulating film;

forming a floating gate electrode separated on a memory cell basis by patterning the control gate electrode material, the interelectrode insulating film, and the floating gate electrode material while forming a control gate electrode arranged on the floating gate electrode in a word line direction; and

forming a gap arranged along the trench in a manner of sinking below the word line between the adjacent floating gate electrode in the word line direction by removing at least a part of the buried insulating film buried in the trench, wherein.

~~16. The method for manufacturing a nonvolatile semiconductor memory device according to claim 15, further comprising forming a cover insulating film stretching over between the control gate electrodes in a manner where the gap is not buried.~~

~~17. The method for manufacturing a nonvolatile semiconductor memory device according to claim 16, further comprising a space formed on the gap between the word lines.~~

~~18. The method for manufacturing a nonvolatile semiconductor memory device according to claim 15, wherein the interelectrode insulating film is formed continuously over the adjacent memory cells in the word line direction in a manner of stretching over the gap.~~

~~19. The method for manufacturing a nonvolatile semiconductor memory device according to claim 15, further comprising covering~~ a word line drawing part in which the word lines drawn out from the memory cells are~~is~~ arranged is covered with a resist upon removing at least a part of the buried insulating film buried in the trench.

7~~20~~. A~~The~~ method for manufacturing a nonvolatile semiconductor memory device ~~according to claim 15~~, ~~further~~ comprising:

depositing a floating gate electrode material on a semiconductor substrate via a tunnel insulating film;

forming a trench in the semiconductor substrate in a bit line direction via the floating gate electrode material and the tunnel insulating film;

forming a buried insulating film in the trench;

forming an interelectrode insulating film on the buried insulating film and the floating gate electrode material;

depositing a control gate electrode material on the interelectrode insulating film;

forming a floating gate electrode separated on a memory cell basis by patterning the control gate electrode material, the interelectrode insulating film, and the floating gate electrode material while forming a control gate electrode arranged on the floating gate electrode in a word line direction;

forming a gap arranged along the trench in a manner of sinking below the word line between the adjacent floating

gate electrode in the word line direction by removing at least a part of the buried insulating film buried in the trench; and

reburying the gap formed in the trench isolating an active area of a bit contact part in which a bit contact is formed with a reburied insulating film after removing at least a part of the buried insulating film buried in the trench.