

PROTECTION CIRCUIT FOR OUTPUT DRIVERS

ABSTRACT

A DRAM output protection circuit (100). A dummy NMOS transistor (116) is connected in parallel with the NMOS output transistor (102). The gate of the dummy transistor (116) is connected through a resistor (122) to ground (108). The resistor 122 value and the gate capacitance (121,127) of the dummy transistor (116) are adjusted to achieve the desired gate matching between the dummy transistor gate (120) and the NMOS output transistor gate (110).

Figure 2

This Sheet Has Been Replaced

