

PATENT SPECIFICATION

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(21) Application No. 47857/77 (22) Filed 17 November 1977

(31) Convention Application No. 2655947

(32) Filed 10 December 1976 in

(33) Federal Republic of Germany (DE)

(44) Complete Specification Published 15 August 1979

(51) INT. CL.² G01R 23/10 H03J 1/02

(52) Index at Acceptance

H3Q 200 6U LX H3H 14B 14D 14G 1A 3D 3G
4D 6A 6B 6D 7A3 7B 7F 7G 8D 8E AK



(54) IMPROVEMENTS IN OR RELATING TO FREQUENCY DETERMINATION

(71) We, LICENTIA PATENT-
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BESCHRANKTER HAFTUNG, a company
organised under the laws of Germany, of
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Germany, do hereby declare the invention,
for which we pray that a patent may be granted
to us, and the method by which it is to be per-
formed, to be particularly described in and by
the following statement:—

This invention relates to the determination
of received frequency in a communications
receiver and is particularly related to the
determination of the frequency for subsequent
digital display.

In communications receiving apparatus,
such as radio apparatus, it is known to indicate
a received frequency by a digital frequency dis-
play or channel indicator instead of an analogue
scale. A typical example of such an apparatus
is described in the periodical "Funkschau"
1976 Vol.9. pp 334-337. Such digital indication
usually relies on the counting of the oscillations,
of the AM or FM local oscillator, by electronic
counters. The oscillations are counted within a
predetermined period called the gating time. In
heterodyne receivers the reception frequency
differs from the local oscillator frequency by
the value of the intermediate frequency (IF).
Thus the IF must be subtracted from (or in
some cases added) to the oscillator frequency.
In a typical circuit this is achieved by pro-
gramming the counting stages of the electronic
counter, prior to counting, to an initial value
such that, after a count equivalent to the IF,
the counter reaches zero counting state. The
following pulses to be counted then give the
received frequency at the end of the counting
time. Thus the counted frequency is corrected
for a fixed and preprogrammed IF value.

In practice, however, it is found that the
fixed value of the IF programmed into the
counter may not exactly agree with the IF value
set by filters included in the IF stage. This
particularly occurs when ceramic filters are

used. These ceramic filters are desirable for
reasons including relatively low cost. They are,
however, trimmed during manufacture and no
subsequent trimming is possible. It is found,
therefore, that the actual value of the IF may
vary for different examples of these filters
and that they cannot be adjusted.

The difference thus obtained could be
corrected by changing the programming of
the counter stages. However they are preferably
programmed prior to installation in the
apparatus and reprogramming is laborious and
expensive and therefore not desirable. Thus
differences do arise between the preprogrammed
IF and that set by the IF filters. This leads to
errors in the displayed frequency. For example,
if the IF value set by the filter is higher than
the programmed value, the indicated reception
frequency will be too high.

It is therefore an object of this invention to
provide an arrangement allowing the correct
indication of frequency despite differences be-
tween the preprogrammed IF value and that set
by the filters.

According to the present invention there is
provided a counting circuit for the determi-
nation of the reception frequency or reception
channel in a heterodyne communications
receiver which includes an AM or FM oscillator
arranged to oscillate at a frequency differing
from the reception frequency by the inter-
mediate frequency of the receiver, the arrange-
ment including an electronic counter arranged
to periodically count the oscillations from the
local oscillator during a gating period and
arranged to subtract from or add to the result
of said count a number of oscillations corres-
ponding to an intended value of the inter-
mediate frequency to be indicative of the
received frequency, or equivalent reception
channel, and control means for varying the
said gating period to compensate the said count
for differences between the intended inter-
mediate frequency and the actual intermediate
frequency of the receiver.

In order that the invention may be clearly understood and readily carried into effect an example thereof will now be described with reference to the accompanying drawings of which:

Figure 1 shows the circuit diagram of a high frequency heterodyne receiver in which the invention is employed, and

Figure 2 shows a part of the circuit of Figure 1 with a practical form for the continuous variation of the gating time.

It has been found that a practical change of the programmed fixed value can also be achieved by changing the gating time. The counting time — and therefore the gating time — covers two periods of time. Firstly, counting is effected from the programmed value up to the zero counting state, the value of the IF being thereby subtracted from the reception frequency. Thereupon, the actual reception frequency is counted, starting from the zero counting state. If now the gating time is somewhat shortened by continuous alteration of its commencement, then the second time interval (in which, after the counting of the programmed fixed value, the counting of the reception frequency begins at the zero counting state) is reduced. Hence a reduced count of the reception frequency is determined. In practice, this is equivalent to a change of programming, since this lower value of the reception frequency would also have been counted if a higher value of the IF had been programmed, with the gating time unaltered.

In Figure 1 the high oscillations received by an antenna 1 are amplified by a high frequency stage 2. In a mixer circuit 3 the received high frequency oscillations are mixed with the oscillations of an oscillator 7, from which results the intermediate frequency IF which is amplified in an intermediate frequency stage which contains the mixer circuit 3. There follow a demodulator 4 and an LF amplifier 5, which latter feeds a loud speaker 6 with the demodulated LF.

In order to represent the reception frequency on an indicating device 11 the oscillations of the oscillator 7 are periodically counted within a gating time T by a counter 10. For this purpose the oscillator 7 is connected to a wideband amplifier 8 which — according to the reception band — amplifies the oscillations of the oscillator either in AM operation or in FM operation. The gating circuit 9 indicates that the counting takes place periodically within the gating time T. By a quartz oscillator 12 pulses 16 are generated the pulse width T of which is equal to the gating time — therefore to the counting time. Via a lead 14 and a further circuit 13 described below in more detail the pulses 16 pass to the gating circuit 9, which is open only during the pulse width T, so that the oscillations of the oscillator can pass from the wideband amplifier 8 to the counter 10

only during the gating time T. The counter 10 is, in the above-described manner, programmed to a value (e.g. 460 kHz for AM and 10.7 MHz for FM) corresponding to the intermediate frequency at the time, whereby the IF is subtracted from the oscillator frequency. The circuit as so far described is with the exception of the circuit 13, known in principle from the reference given hereinbefore. The count displayed on indicator 11 can if desired be further modified to represent a channel number rather than frequency.

As can be seen from the lower part of Figure 1, the gating time is formed by negative pulses 16. During the gating time T the voltage level is e.g. -5V, and during the other time is 0V. It will now be assumed that the counter 10 is programmed to a value corresponding to the IF of 10.7 MHz. The filter incorporated in the IF stage as a component and already trimmed, e.g. a ceramic filter or a quartz filter (not illustrated) may however have a somewhat higher IF, e.g. 10.8 MHz. With an assumed gating time T of 8 msec and a reception frequency of for example 100 MHz, without the invention the reception frequency would be determined by the counter 10 too high by e.g. 100 kHz. This is because, owing to the programming being lower than to the actual intermediate frequency of the IF stage 3, the value subtracted from the oscillator frequency would be too low and then the reception frequency indicated will be correspondingly high.

In order to eliminate this error, in the circuit 3, which will be explained in more detail below with reference to Figure 2, means are provided which permit a continuous change of the pulse width of the pulses 16. As can be seen from Figure 1, the circuit 13 has the effect that the leading flank 16a of the pulses 16 fed to the gating circuit 9 via the lead 15 is delayed by the time ΔT . The gating circuit 9 is thus opened for a shorter time than the original time T, by the time ΔT , so that the actual counting time of the counter 10 is reduced. Accordingly, fewer oscillations than previously are counted. This means, however, that instead of the value of the reception frequency being too high, as discussed above, the correct lower value is counted, if the period of time ΔT is suitably selected. In the example given the error of 100 kHz is eliminated by $\Delta T = 8 \mu\text{sec}$. Thus by continuous alteration of the actual gating time T — ΔT , matching of the IF value determining the counting to the IF of the filter employed in the IF stage is achieved.

In Figure 2 there is illustrated a part of the circuit of Figure 1, with a practical example of the circuit 13. Parts corresponding to one another in Figure 1 are provided with the same references. The oscillations of the oscillator pass via divider stages 17 and 18 to a frequency counter 19, to which the gating time pulses 16 generated by the quartz

oscillator 12 are fed. The frequency counter 19 is for example constructed as a MOS-IC and also includes the control circuit necessary for the whole counting operation, as well as an encoding circuit for the 7-segment indicator 11, on which the reception frequency is to be indicated. As the frequency indicator 19 there may for example be used the MOS-IC DFU 101 described in the reference.

The dividers 17 and 18 are constructed in TTL technique. For the divider 17 there may be considered for example type SN 7490, and for the divider 18 type SN 7474.

The circuit 13 for shifting the beginning of the gating time T includes a potentiometer 24, a resistor 23, a diode 21 and a capacitor 22. The potentiometer 24 is connected via a terminal 25 to a voltage of 0V, and via another terminal 26 to -5V. The variable tapping of the potentiometer 24 leads via the resistor 23 to the capacitor 22, which is thereby charged to an adjustable negative voltage. Owing to the pulses 16 occurring at the output terminal 31 of the frequency counter 19 the counter 22 is discharged at the beginning of the gating time T via the diode 21. As a result, the delay of T of the flank 16a, shown by a broken line at the bottom right-hand part of Figure 1, occurs and with it the beginning of the actual gating time (T- ΔT). The diode 21 has the effect that only the beginning of the gating time is delayed, the end of the gating time remaining uninfluenced. After the end of the gating time, when the pulse jumps from -5V to 0V, the condenser is again charged to the original value, so that during the next gating time pulse the delay of the beginning of the gating time the ΔT , caused by the discharge, again occurs. The magnitude of the delay ΔT depends on the extent of pre-charging of the condenser 22. By varying the tapping of the potentiometer 24 the extent of pre-charging of the condenser 22 and therewith the magnitude of the delay ΔT may be adjusted. Thus the magnitude of the IF deviation can be adjusted in a simple manner by actuation of the potentiometer 24; in the arrangement of Figure 2 however only an increase from a predetermined, preselected value is possible. A resistor 20 serves as external resistor for a switching transistor located in the frequency counter at the point 31, which connects to 0V outside the gating time.

The pulses 16, which have been shortened in the manner described, pass via an inverter 28 to an input E (enable) of the divider 18 and, via a further inverter 29, to an input R (reset) of the divider 17. The effect of this control of the dividers 17 and 18 is that they are in operation only during the gating time, so that the counting operation can take place only periodically within the gating time. The inverter 28, which for example is of type 7404, includes an internal diode 30, which is

illustrated in Figure 2 in broken lines. This diode is of importance to the extent that the logical voltage levels for the MOS-IC and for the TTL circuits 17, 18 are different. The voltage of -5V corresponds to the logical level "0" in TTL technique, and the voltage 0V to the logical level "1". By means of the internal diode 30 a fall of voltage below the value -5V (TTL "0") is achieved. When the voltage level falls below -5V, in fact, the internal diode 30 becomes conducting and therefore prevents a further fall of voltage.

In the practical example in Figure 2 the gating time is altered continuously. It is however also possible to delay the beginning of the gating time by discrete steps, and/or to make the change reversible, for example in order to enable different deviations of the IF in different bands to be compensated. For this purpose, instead of the potentiometer, fixed voltage dividers may be provided and in some cases reversed or a plurality of potentiometers may be provided and reversed as regards the tapping point.

The invention may be used in advantageous manner particularly in the VHF band, since here no ceramic filters of sufficient IF accuracy are present and consequently deviations of the filter IF from the programmed IF of the counting circuit frequently occur.

WHAT WE CLAIM IS:-

1. A counting circuit for the determination of the reception frequency or reception channel in a heterodyne communications receiver which includes an AM or FM local oscillator arranged to oscillate at a frequency differing from the reception frequency by the intermediate frequency of the receiver, the arrangement including an electronic counter arranged to periodically count the oscillations from the local oscillator during a gating period and arranged to subtract from or add to the result of said count a number of oscillations corresponding to an intended value of the intermediate frequency to be indicative of the received frequency, or equivalent reception channel, and control means for varying the said gating period to compensate the said count for differences between the intended intermediate frequency and the actual intermediate frequency of the receiver.

2. A counting circuit according to claim 1, wherein the gating period is determined by the pulse width of periodically generated pulses (16), and the control means reduces the pulse width by shifting the flank that determines the beginning of the gating time.

3. A counting circuit according to claim 2, wherein the pulses are negative and including a capacitor, receiving the pulses, which is charged via a control resistance, and is discharged during the gating time so that the flank determining the beginning of the gating time is delayed.

4. Counting circuit according to claim 3

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oscillator 12 are fed. The frequency counter 19 is for example constructed as a MOS-IC and also includes the control circuit necessary for the whole counting operation, as well as an encoding circuit for the 7-segment indicator 11, on which the reception frequency is to be indicated. As the frequency indicator 19 there may for example be used the MOS-IC DFU 101 described in the reference.

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55 The pulses 16, which have been shortened in the manner described, pass via an inverter 28 to an input E (enable) of the divider 18 and, via a further inverter 29, to an input R (reset) of the divider 17. The effect of this control of the dividers 17 and 18 is that they are in operation only during the gating time, so that the counting operation can take place only periodically within the gating time. The inverter 28, which for example is of type 7404, includes an internal diode 30, which is

illustrated in Figure 2 in broken lines. This diode is of importance to the extent that the logical voltage levels for the MOS-IC and for the TTL circuits 17, 18 are different. The voltage of -5V corresponds to the logical level "0" in TTL technique, and the voltage 0V to the logical level "1". By means of the internal diode 30 a fall of voltage below the value -5V (TTL "0") is achieved. When the voltage level falls below -5V, in fact, the internal diode 30 becomes conducting and therefore prevents a further fall of voltage.

In the practical example in Figure 2 the gating time is altered continuously. It is however also possible to delay the beginning of the gating time by discrete steps, and/or to make the change reversible, for example in order to enable different deviations of the IF in different bands to be compensated. For this purpose, instead of the potentiometer, fixed voltage dividers may be provided and in some cases reversed or a plurality of potentiometers may be provided and reversed as regards the tapping point.

The invention may be used in advantageous manner particularly in the VHF band, since here no ceramic filters of sufficient IF accuracy are present and consequently deviations of the filter IF from the programmed IF of the counting circuit frequently occur.

WHAT WE CLAIM IS:-

1. A counting circuit for the determination of the reception frequency or reception channel in a heterodyne communications receiver which includes an AM or FM local oscillator arranged to oscillate at a frequency differing from the reception frequency by the intermediate frequency of the receiver, the arrangement including an electronic counter arranged to periodically count the oscillations from the local oscillator during a gating period and arranged to subtract from or add to the result of said count a number of oscillations corresponding to an intended value of the intermediate frequency to be indicative of the received frequency, or equivalent reception channel, and control means for varying the said gating period to compensate the said count for differences between the intended intermediate frequency and the actual intermediate frequency of the receiver.

2. A counting circuit according to claim 1, wherein the gating period is determined by the pulse width of periodically generated pulses (16), and the control means reduces the pulse width by shifting the flank that determines the beginning of the gating time.

3. A counting circuit according to claim 2, wherein the pulses are negative and including a capacitor, receiving the pulses, which is charged via a control resistance, and is discharged during the gating time so that the flank determining the beginning of the gating time is delayed.

4. Counting circuit according to claim 3

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- in which the control resistance is an adjustable resistor.
- 5 5. A counting circuit according to either of claims 3 or 4 wherein the negative pulses are fed to the capacitor via a diode poled so that the flank of the pulse determining the end of the gating time is not influenced.
- 10 6. A counting circuit according to any of claims 2 to 5, including a frequency counter and divider stages via which the pulses of reduced width are applied to the counter.
- 15 7. A counting circuit according to claim 3, wherein the control resistance is at least one fixed voltage divider.
8. A counting circuit according to claim 7, wherein a plurality of fixed voltage dividers are provided and are made reversible by commutators.
9. A counting circuit according to claim 8
- in which the commutators are situated at the tapping points of the dividers.
- 20 10. A counting circuit according to claim 4, wherein a plurality of adjustable resistors are provided and are made reversible by commutators.
- 25 11. A counting circuit according to claim 4 in which the commutators are situated at the tapping point of the resistors.
- 30 12. A counting circuit substantially as herein described with reference to the accompanying drawings.
13. A heterodyne communications receiver including a counting circuit according to any of the preceding claims.
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