

SPECIFICATION

Divide-by-two charge divider

5 The invention relates to a device for the division of an electric charge into equal halves, for use in analog-to-digital or digital-to-analogue converters, employing clock pulse controlled charge transfer devices.

10 The IEEE JI. SSC of December 1975, page 371 *et al* and December 1976, page 722 *et al*, described devices for analog-to-digital (ADC) and digital-to-analog (DAC) conversion, in which it is attempted to repeatedly divide a charge into halves by means of a series of capacitors with binary weighted values. This presents problems in accurately realising the correct capacitance values, which is decisive for the accuracy with which the relevant charge division is effected.

20 The invention is characterised in that said electric charge is distributed between two parallel branches, which branches each comprise a charge transfer device and a storage capacitance, which capacitances can each acquire half the said electric charge by means of the related charge transfer device with an inaccuracy which is determined by the inequality of the charge transfer devices, each of the storage capacitances being coupled to a respective two further alternately operative charge transfer devices, of which one further device transfers the charge stored in the storage capacitance of one of said branches to a collecting capacitance situated in the same branch, whilst the other one of the further charge transfer devices transfers said charge to a collecting capacitance situated in the other branch.

35 The invention is based on the concept that for converting a digital signal into an analog signal with the aid of a charge transfer device (CTD), such as a bucket brigade device (BBD) or a charge coupled device (CCD), it is simply possible to distribute charges among parallel branches with for example equal capacitors (known *per se* from IBM Techn. Disc. Bull., January 1976, page 2540) and to obtain a series of binary weighted charges according to this principle. The charges of this series, of which the bit corresponding weight of the digital input signal is for "1", are added so that an overall charge is obtained which is the analog equivalent of the digital signal. For the conversion of analog signals into digital signals the output of a DAC as described in the foregoing may be compared with the analog input signal and from the difference of the two the digital control of the charge transfer devices may be derived, which then yields the digital signal.

55 A major advantage of the use of parallel branches in comparison with the prior art known from the aforementioned articles in IEEE JI. SSC., is that now if desired, capacitors with equal or nearly equal capacitance values may be used, so that the number of bits of the DAC or ADC, in comparison with the said known devices, could be extended substantially. However, the conversion accuracy then also remains dependent on the accuracy with which the charge transfer devices in the two parallel branches are identical to each other. However, said inequality

has no consequences owing to the use of the aforementioned further charge transfer devices, as will become apparent hereinafter.

The invention will now be described in more detail by way of example with reference to the accompanying drawings, in which:—

Figure 1 shows a device which illustrates the principle of the invention;

Figure 2 represents voltage-time diagrams of the clock pulses employed in Figure 1 and,

Figure 3 illustrates the combination of devices in accordance with Figure 1 to form a digital-to-analog converter.

In the device of Figure 1 a source of constant voltage V_0 charges a capacitor C_0 via a transistor 1 which is controlled by a clock pulse ϕ_1 , and which is specifically an insulated gate field-effect transistor (IGFET), so that a given reference charge Q is stored in the capacitor C_0 . By means of a charge transfer device, in this case a transfer gate, comprising a transistor 2 controlled by a clock pulse ϕ_2 , most of this charge Q is transferred to a storage capacitance C_1 , from which it is applied to two parallel branches A and B, respectively, each comprising an isolating transistor 3a and 3b, respectively, operated in cascade, a transfer gate, comprising a transistor 4a and 4b, respectively, and a storage capacitance C_{2a} and C_{2b} , respectively. The transistors 4a and 4b are also controlled by the clock pulse ϕ_1 . If the transistors 3a and 3b and 4a and 4b had exactly the same properties, specifically the same threshold voltages and channel resistances (the capacitances C_{2a} and C_{2b} need not be exactly equal), then at the instant at which by means of the clock pulse ϕ_1 the charge Q on the capacitance C_1 is transferred to the capacitances C_{2a} and C_{2b} , via the transistors 4a and 4b, respectively, each of the last-mentioned capacitances would acquire exactly the charge $\frac{1}{2}Q$. However, in practice this requirement cannot be met, especially not by means of an integrated circuit version, where it is already difficult to obtain mutual property differences below 1%.

Via isolating transistors 5a and 5b, respectively, which are operated in cascode, the capacitances C_{2a} and C_{2b} , in accordance with the further characteristic feature of the invention, are followed by a respective two transfer gates comprising transistors 6a and 7a and 6b and 7b, respectively, and collecting capacitances C_{3a} and C_{3b} , respectively. Clock pulses ϕ_3 and ϕ_4 , applied to these transfer gates, and the clock pulse ϕ_2 which is simultaneously applied to the lower side of the capacitances C_{3a} and C_{3b} , respectively, ensure that either the transfer gates 6a and 6b or the transfer gates 7a and 7b are operative. (Thus, in contradistinction to the said article in IBM-TDB no direct connection is established between the upper sides of the capacitances C_{2a} and C_{2b}). As a result of this, the charges on the capacitances C_{2a} and C_{2b} are transferred to the collecting capacitances C_{3a} and C_{3b} , respectively, during the clock pulse phase ϕ_3 , and to the collecting capacitances C_{3b} and C_{3a} , respectively, during the clock pulse phase ϕ_4 . If the first-mentioned charges are $\frac{1}{2}Q(1+x)$ and $\frac{1}{2}Q(1-x)$ respectively, in which x represents the charge deviation as a result of the inequality of the transfer and

isolating transistors specifically of the transistors 3a and 4a, respectively, and 3b and 4b, respectively, each of the collecting capacitances C3a and C3b will alternately receive the charges $\frac{1}{2}Q(1+x)$ and $\frac{1}{2}Q(1-x)$.

- 5 The capacitance C3a, via an isolating transistor 8a operated in cascode, is connected to a transfer gate comprising a transistor 9a connected to a storage capacitance C4a, which is also controlled by the clock pulses ϕ_1 . Thus, the sum of the two above-mentioned charges, i.e. a charge Q, will be transferred to the capacitance C4a.

Thus, the steps described so far apparently seem to have no effect, because from the reference charge Q on the capacitance C₁ an equal charge on the capacitance C4a has been derived. However, from the following it will appear that actually some progress is made. The capacitance C3b, in its turn, is followed by two parallel branches B' and C which are identical to the branches A and B, i.e. the capacitance C3b is connected to transfer gates via isolating transistors 8b and 8c, respectively, which correspond to the previously described transistors 3a and 3b, respectively, which transfer gates comprise transistors 9b and 9c (corresponding to the transistors 4a and 4b, respectively) and are connected to storage capacitances C4b and C4c, respectively (corresponding to capacitances C2a and C2b, respectively) etc. This is schematically represented in Figure 3.

In this Figure the block 1, 2 corresponds to the circuit elements 1 and 2 of Figure 1, by means of which the charge Q is derived from the voltage V_0 . The branches 4a and 4b, corresponding to the relevant transfer gates of Figure 1, divide said charge into approximately equal halves $\frac{1}{2}Q$, whilst the branches 6a, 6b, 7a and 7b correspond to the relevant "further" transfer gates of Figure 1. If the errors introduced in the charge division by the gates 3a, 4a, 3b, 4b and 8b, 9b, 8c, 9c, are x_1 and x_2 , respectively, a charge $\frac{1}{2}Q(1+x_1)$, say, will arrive at the capacitance C3b during the clock pulse phase ϕ_2 and a charge $\frac{1}{2}Q(1-x_1)$ during the clock pulse phase ϕ_4 . Under the influence of the clock pulse ϕ_1 on the transfer gates 9b and 9c, this charge is again divided into approximately equal halves with an error x_2 , so that during the clock pulse phase ϕ_3 a charge $\frac{1}{4}Q(1+x_1-x_2)$ will arrive at the capacitance C4b, and a charge $\frac{1}{4}Q(1+x_1+x_2)$ at the capacitance C4c, whilst during the clock pulse phase ϕ_4 a charge $\frac{1}{4}Q(1-x_1-x_2)$ will arrive at the capacitance C4b and a charge $\frac{1}{4}Q(1-x_1+x_2)$ at the capacitance C4c. The transfer gates 10b, 11b and 10c, 11c, respectively, (corresponding to the transfer gates 6a, 7a and 6b, 7b, respectively) following said capacitances ensure that during the clock pulse phase ϕ_3 the charges then present are further transferred alternately. The result is that the charges $\frac{1}{4}Q(1+x_1-x_2)$ and $\frac{1}{4}Q(1-x_1+x_2)$ are collected the capacitance C5b and then transferred to the storage capacitance C6b of the branch B': thus an error free $\frac{1}{2}Q$ is obtained (when ignoring second-order effects).

In a similar way the branch C is followed by two further parallel branches (corresponding to the branches B' and C) etc., by means of which error free charge values $Q/4$, $Q/5$, etc., can be obtained. These charges are applied to a summing device S control-

led by a digital input signal DI, which device S comprises a plurality of electronic two-way switches, each of which depending on the value of the signal DI transfers the relevant charge either to the analog output A0 or to earth. (In Figure 1 one of these two-way switches is represented by the transistors 13 and 14, the clock pulse ϕ_2 being applied to the transistor 13 or 14 depending on the value of the signal DI).

75 Where in the foregoing there is mention of capacitances, it will be evident that for these capacitances it is possible to utilise internal capacitances of a semiconductor body, such as occur in CCD's, PCCD's, etc.

The use of IGFET's operated in cascode, (2, 3a, 3b, 5a, 5b, etc.), i.e. the source electrode used as input (on the left in the Figure), the gate electrode at a fixed potential (earth) and the drain electrode as output (on the right in the Figure), has the advantage of a better charge transfer efficiency: the cascode IGFET's 5a, 5b, etc., preceding the "further" charge transfer devices moreover have the advantage that any errors introduced by, for example, threshold voltage differences of the transistors 6a and 7a, or 6b and 7b, are avoided. The charge transferred from the capacitance C2a to the respective capacitances C3a and C3b by the transfer gates 6a and 7a, respectively then virtually depends only on the threshold voltage of the transistor 5a and is no longer influenced by the efficiency of the transfer gates 6a and 7a, respectively. The same applies in respect to the capacitance C2b, transistor 5b and transfer gates 6b and 7b.

In general, the steps described will be mainly applied to the more significant bits of a digital-to-analog converter, because for the less significant bits, i.e. the bits which differ by a great division factor from the charge Q, the said errors are no longer of significance.

CLAIMS

105 1. A device for the division of an electric charge into equal halves, for use in analog-to-digital or digital-to-analog converters, employing clock-pulse controlled charge-transfer devices, characterised in that said electric charge is distributed between two parallel branches, which branches each comprise a charge transfer device and a storage capacitance, which capacitances can each acquire half the said electric charge by means of the related charge transfer device with an inaccuracy which is determined by the inequality of the charge transfer devices, each of the storage capacitances being coupled to a respective two further alternately operative charge transfer devices, of which one further device transfers the charge stored in the storage capacitance of one of said branches to a collecting capacitance situated in the same branch, whilst the other one of the further charge transfer devices transfers said charge to a collecting capacitance situated in the other branch.

125 2. A device as claimed in Claim 1, characterised in that at least the further charge-transfer devices are preceded by transistors operated in cascode.

130 3. A device for the division of an electric charge into equal halves substantially as hereinbefore described with reference to Figures 1 and 2 of the accompanying drawings.



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125 2. A device as claimed in Claim 1, characterised in that at least the further charge-transfer devices are preceded by transistors operated in cascode.

130 3. A device for the division of an electric charge into equal halves substantially as hereinbefore described with reference to Figures 1 and 2 of the accompanying drawings.



(16)

4. An arrangement for the repeated division of an electric charge into equal halves for producing binary weighted charges, substantially as hereinbefore described with reference to Figure 3 of the accompanying drawings.
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