DUAL SILICON-ON-INSULATOR DEVICE WAFER DIE

TECHNICAL FIELD

The present invention relates generally to silicon-on-insulator devices and more particularly to integration of partially and fully depleted silicon-on-insulator devices on a single wafer die.

BACKGROUND ART

Silicon-on-insulator (SOI) devices have often been dubbed as the next successor to the reigning complimentary metal-on-silicon (CMOS) field effect transistors (FET) devices. SOI device advantages include excellent isolation protection against cross-talk, almost null leakage, latch-up immunity, radiation hardness, reduced junction capacitance, and reduced junction leakage currents. In addition, fully depleted SOI devices offer additional advantages. They provide reduced short channel effect, near ideal sub-threshold slope, increased transconductance, and reduced threshold voltage (V_t) sensitivity to changes in body doping, channel length, temperature, and substrate voltage. Fully depleted SOI devices are those in which the layer of semiconductor is sufficiently thin that the entire thickness of the body region is depleted of majority carriers when in the off state and both diffusion junctions are at ground.

In some CMOS FET devices, n-channel MOS transistors are coupled to a complimentary p-channel MOS transistor to provide an integrated circuit having very low power requirements.

The capability of having both partially and fully depleted SOI devices on the same wafer die has not previously been possible. Further, the possibility of making either PMOS or NMOS devices of either the partially depleted or fully depleted SOI devices has also not previously been possible.

A system for integrating both partially depleted and fully depleted SOI devices and PMOS and NMOS devices within a single die has long been sought, but has long eluded those skilled in the art.

DISCLOSURE OF THE INVENTION

The present invention provides a silicon-on-insulator semiconductor device in which a single wafer die contains a transistor in a silicon island over an insulator layer to form a fully depleted silicon-on-insulator device and a transistor formed in a semiconductor island over an insulator structure to form partially depleted silicon-on-insulator devices.

The present invention further provides a manufacturing method for having both partially and fully depleted silicon-on-insulator field effect transistor devices on the same wafer die, and a system for integrating either PMOS or NMOS devices of either the partially depleted or fully depleted silicon-on-insulator field effect transistor devices within a single die by using conventional doping processes.

The above and additional advantages of the present invention will become apparent to those skilled in the art from a reading of the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a single wafer die with a semiconductor substrate having an oxide layer with an opening thereon;

FIG. 2 is the structure of FIG. 1 with a liner oxide covering the oxide layer and semiconductor substrate;

FIG. 3 is the structue of FIG. 2 with a nitride spacer deposited over the liner oxide;

FIG. 4 is the structure of FIG. 3 showing the oxide structure formed after the step of thermal oxidation;

FIG. 5 is the structure of FIG. 4 after the nitride and liner oxide have been removed exposing the oxide layer and portions of the semiconductor substrate;

FIG. 6 is the structure of FIG. 5 after the silicon epitaxial growth (selective and non-selective) layer is added;

FIG. 7 is the structure of FIG. 6 with a nitride layer and an oxide layer deposited thereon to protect the active silicon and act as an oxide chemical-mechanical polishing stop layer;

FIG. 8 is the structure of FIG. 7 after masking and dry etching the silicon epitaxial growth layer into silicon islands;

FIG. 9 is the structure of FIG. 8 after oxide deposition and chemical-mechanical polishing; and

FIG. 10 is the structure of FIG. 9 showing a partially depleted silicon-on-insulator field effect transistor device disposed between two fully depleted silicon-on-insulator devices.

BEST MODE FOR CARRYING OUT THE INVENTION

Referring now to FIG. 1, therein is shown a single wafer die 10 shown in an intermediate state of completion. A semiconductor substrate 12 of a semiconductor material such as silicon has had an insulator material such as an oxide layer 14 deposited thereon. The oxide layer 14 has been coated with a photoresist (not shown), the photoresist has been patterned and developed, the oxide layer 14 has been etched, and the photoresist has been removed to leave the oxide layer 14 with an opening 16 of about 0.5 μm to 10 μm provided therein.

Referring now to FIG. 2, therein is shown the structure of FIG. 1 after deposition of a liner insulator such as a liner oxide 18. The liner oxide 18 is a conformal layer in a thickness of about 100 Å to 500 Å which covers the oxide layer 14 and the semiconductor substrate 12.

Referring now to FIG. 3, therein is shown the structure of FIG. 2 having an insulator having a different selectivity from the oxide layer 14 such a nitride layer (not shown) of a thckness of about 200 Å to 1000 Å deposited thereon which is formed into a nitride spacer 20 over a portion of the semiconductor substrate 12. The nitride spacer 20 is formed by depositing the nitride layer over the liner oxide 18 and isotropically etching it until only the nitride spacer 20 remains to protect the sidewalls of the liner oxide 18 and a portion of the bottom adjacent to the semiconductor substrate 12.

Referring now to FIG. 4, therein is shown the structure of FIG. 3 after a thermal processing or thermal oxidation. The thermal oxidation causes a growth of the liner oxide 18 on the semiconductor substrate 12 to form an insulator structure such as an oxide structure 22. The thermal oxidation at 800°C to 950°C for a few minutes in a furnace can be a wet oxidation in an O_2 and H_2O ambient or can be a partially wet oxidation in an O_2, H_2O and H_2 ambient.

Referring now to FIG. 5, therein is shown the structure of FIG. 4 after a nitride removal step and an oxide strip step. In the nitride removal step, the nitride spacer 20 is etched away by a wet etch process using H_3PO_4 and then the liner oxide 18 is removed in an

oxide strip which eliminates the oxide liner 18 and reduces the size of the oxide structure 22 to result in an oxide structure 24. At this point the oxide layer 14 and portions of the semiconductor substrate 12 are exposed.

Referring now to FIG. 6, therein is shown the structure of FIG. 5 after growth of an insulator silicon epitaxial growth (SEG) layer or silicon layer 26. The silicon layer 26 can be grown in two stages with a first by selective epitaxial growth and the second by non-selective epitaxial growth. The silicon layer 26 covers the oxide layer 14, portions of the semiconductor substrate 12, and the oxide structure 24 to a controlled depth to be the silicon portion of the field effect transistor (FET) devices.

Referring now to FIG. 7, therein is shown the structure of FIG. 6 having protective insulator layers of an oxide layer 28 and a nitride layer 30 deposited thereon. The oxide layer 28 is generally deposited to a thickness of approximately 100 Å and the nitride layer 30 is generally deposited to a thickness of about 1000 Å to 2000 Å.

Referring now to FIG. 8, therein is shown the structure of FIG. 7 after masking and dry etching of the silicon layer 26. The structure of FIG. 7 has a photoresist (not shown) deposited thereon, the photoresist patterned, and developed. The nitride layer 30, the oxide layer 28 and the silicon layer 26 are then dry etched to form the openings 32, 34, 36, and 38 of about 0.35 μm to 10 μm which define silicon islands 26', 26'', and 26'''.

Referring now to FIG. 9, therein is shown the structure of FIG. 8 after deposition of an insulator oxide and oxide chemical-mechanical polishing (CMP). A chemical vapor deposition (CVD) process is preferably used to deposit an oxide layer over the structure shown in FIG. 8. A oxide CMP is performed and the nitride layer 30 and the oxide layer 28 act as a CMP stop layer to protect the silicon islands 26', 26'', and 26''' from damage during the oxide CMP. The oxide CMP leaves the oxide layer 40 in the previous openings 32, 34, 36, and 38 and isolates the silicon islands 26', 26'', and 26'''.

Referring now to FIG. 10, therein is shown the completed single wafer die 10 with gate oxides 42 in a thickness of about 10 Å to 100 Å preferably thermally grown over the silicon islands 26', 26'', and 26''' and the implantations performed to form the diffusion junctions 44.

In FIG. 10, the silicon islands 26' and 26'' on the insulator oxide layer 14 form two fully depleted silicon-on-insulator (SOI) devices 46 and the silicon island 26'' on the insulator oxide structure 24 forms a partially depleted SOI device 48. By using conventional doping processes to implant p- and n-type dopants into the silicon islands 26'or 26'', either

the partially depleted or the fully depleted SOI device 46 or 48 can be formed into a PMOS or an NMOS device. This gives full flexiblity of design to an integrated circuit designer to make the components desired in all different combinations.

While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations which fall within the spirit and scope of the included claims. All matters set forth herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

THE INVENTION CLAIMED IS:

1. A method for making a silicon-on-insulator semiconductor device [46] comprising:

providing a semiconductor substrate [12];

depositing an insulator layer [14] on the semiconductor substrate [12];

forming an opening [16] in the insulator layer [14];

forming an insulator structure [24] in a portion of the opening [16] on the semiconductor substrate [12];

forming silicon [26] on the insulator structure [24] and the insulator layer [14];

forming openings [32,34,36,38] in the silicon [26] to form silicon islands [26',26'',26'''];

depositing insulator [40] in the openings [32,34,36,38];

forming gate insulators [42] on the silicon islands [26',26'',26'''']; and

forming junctions [44] in the silicon islands [26',26'',26''''].

2. The method as claimed in claim 1 wherein forming the insulator structure [24] includes:

depositing a liner oxide layer [18];

depositing a spacer layer [20];

forming a spacer [20] on a portion of the liner oxide layer [18] in the opening [16] in the insulator layer [14]; and

growing the insulator structure [24] by thermal oxidation of the liner oxide layer [18] not under the spacer [20].

3. The method as claimed in claim 2 wherein forming the insulator structure [24] includes:

depositing a spacer layer [20] of a nitride [20]; and

isotropically etching the nitride [20] to form a nitride spacer [20].

4. The method as claimed in claim 1 wherein forming openings [32,34,36,38] in the silicon [26] includes:

depositing an oxide layer [18] on the silicon [26];

depositing a nitride layer [20] on the oxide layer [18];

depositing, patterning, and developing a photoresist;

etching the nitride layer [20];

etching the oxide layer [18]; and

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etching the silicon [26].

5. The method as claimed in claim 1 wherein depositing the insulator [40] in the openings [32,34,36,38] in the silicon [26] includes:

depositing an oxide layer [18] on the nitride layer[26''], on the insulator layer [14], on the insulator structure [24], and on the semiconductor substrate [12]; and

chemical mechanical polishing the oxide layer [18] to be coplanar with the silicon [26].

6. The method as claimed in claim 1 wherein forming gate insulators [42] on the silicon islands [26',26'',26'''] includes depositing a gate oxide [42] on the silicon islands [26',26'',26'''] and the insulator [40] in the openings [32,34,36,38] and removing the gate oxide [42] on the insulator [40] in the openings [32,34,36,38] and on a portion of the silicon islands [26',26'',26'''].

7. The method as claimed in claim 1 wherein forming the gate insulator [42] on and the junctions [44] in the silicon island [26''] over the insulator structure [24] forms a partially depleted silicon-on-insulator device [48].

8. The method as claimed in claim 1 wherein forming the gate insulator [42] on and the junctions [44] in the silicon island [26',26'''] over the insulator layer [14] forms a fully depleted silicon-on-insulator device [46].

9. The method as claimed in claim 1 wherein forming the gate insulator [42] on and the junctions [44] in the silicon island [26',26'',26'''] forms a P-channel silicon-on-insulator transistor [46,48].

10. The method as claimed in claim 1 wherein forming the gate insulator [42] on and the junctions [44] in the silicon island [26',26'',26'''] forms an N-channel silicon-on-insulator transistor [46,48].

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