

PATENT SPECIFICATION (11)

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(54) METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES

(71) We, EASTMAN KODAK COMPANY, a Company organized under the Laws of the State of New Jersey, United States of America, of 343 State Street, Rochester, New York 14650, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a method of manufacturing semiconductor devices and, more particularly, to an improved method of manufacturing semiconductor devices provided with extremely flat, thin polysilicon overcoats.

In recent years solid state semiconductors of the type known as charge transfer devices have been utilized in a growing number of imaging devices. A charge transfer device adapted for use in an imaging device typically comprises a suitably doped wafer (chip), a silicon dioxide coating on the wafer, and transparent electrodes overlying the silicon dioxide coating. Preferably the transparent electrodes are formed of doped polycrystalline silicon (polysilicon) which is intrinsically compatible with the silicon dioxide coating.

In one known prior art procedure for forming a polysilicon overcoat, a silicon wafer having a coating of silicon dioxide thereon is exposed to reactant gases at an elevated temperature which blow past the wafer and, in so doing, cause a polysilicon coating to form on the silicon dioxide coating. One disadvantage of this procedure is that the upstream portion of the silicon wafer gets more thickly coated with polysilicon than does the downstream portion, causing

the polysilicon coating to taper in thickness. Such tapering has certain disadvantages: (1) tapering causes "variable" fringing effects to occur across the face of the imaging device; (2) tapering causes variable sensitivity, both monochromatic and spectral, across the plane of the imaging device, i.e., from imaging element to imaging element. Also, even ignoring the tapering effects, chemical vapour deposition is not a tightly controllable practice, and results in batch-to-batch polysilicon thickness variations.

U.S. Patent No. 3,465,428 discloses a method of fabricating thin film semiconductor devices by vacuum depositing cadmium sulphide and other polycrystalline semiconductor powders to form a thin polycrystalline coating on an ohmic contact layer previously deposited on a substrate. Polycrystalline silicon is not specifically mentioned in the specification. However, when the procedure suggested in U.S. Patent No. 3,465,428 was used to form polysilicon coatings, i.e. by vacuum deposition of polysilicon on the silicon semiconductor chip employing polysilicon as the evaporant, coatings having relatively large (as compared to the coating thickness) lumps of polysilicon across the surface of the chip were produced. Such chips are useless in an imaging device.

In accordance with the present invention there is provided a method of forming a polysilicon coating on a semiconductor device, said method comprising the steps of evaporating monocrystalline silicon in a vacuum chamber, exposing the semiconductor device to the silicon vapour, thereby depositing amorphous silicon on the semiconductor device, and heating the semiconductor device to a temperature sufficient to crystallize said

amorphous silicon.

In accordance with the present invention there is also provided a semiconductor device formed by the method set out in the immediately preceding paragraph.

The present invention will now be described by way of example with reference to the accompanying drawings in which:—

Figure 1 is a schematic diagram of a vacuum deposition system used in the practice of the present invention; and

Figure 2 is a flow diagram identifying post deposition procedures for practising the present invention.

Referring to Fig. 1, a vacuum chamber 10 cooperates with an evaporation unit 12, the evaporation unit 12 being connected to a vacuum source 14 capable of providing a chamber vacuum of, say, 5×10^{-6} torr. A pedestal 16 within the evaporation unit 12 supports a crucible 18. An electron source 20 connected to electronics unit 12 spews high energy electrons through a window 24. Electrons emitted by the source 20 are directed by a magnetic field 26 to the interior of the crucible 18, causing the contents therein to boil.

A shutter 28, having a chute 30 therein, may be actuated by a shutter control 32 to shut off, or not, source vapour from reaching silicon wafers 34 to be coated. The wafers 34 are mounted to wheels 36 which rotate (by means not shown) to assure even coatings on the wafers 34.

A quartz crystal 38 aligns with the chute 30 and, as the crystal 38 gets coated with the evaporant, its resonant frequency changes, signalling a measure of coating thickness to "resettable" thickness control electronics 40.

In first attempting to vacuum deposit polysilicon on silicon wafers 34, several chunks of polysilicon were placed in the crucible 18 and electron-beam heated. After the crystal 38 and thickness control electronics 40 registered the desired coating thickness, the shutter 28 was actuated to shield the wafers 34 from additional coating. Then the wafers 34 were examined, revealing relatively large (as compared to the coating thickness) lumps of polysilicon across the wafer surfaces. In seeking an explanation for these defects, it was postulated that polysilicon, as a result of its formation, perhaps includes tiny gas bubbles trapped within its structure . . . and that such gas bubbles erupted at the surface of the boiling polysilicon and effectively splattered polysilicon in the direction of the coated surfaces of the silicon wafers 34. Corollarily, it was reasoned that monocrystalline silicon -- by virtue of the squeezeing influence of silicon atoms which align to form a monocrystalline silicon structure -- would probably include few, if any, trapped gas bubbles. thus several chunks of monocrystalline silicon were

placed in the crucible 18 and used as the evaporant.

After the crystal 38 and thickness control electronics 40 registered the desired coating thickness, the shutter 28 was actuated to shut off the vacuum deposition. The coating was then examined and revealed an extremely thin coating which was everywhere within $\pm 20 \text{ \AA}$ of the target thickness.

The silicon coating formed by vacuum deposition, whether of poly- or monocrystalline silicon, is an amorphous one. As shown in Fig. 2, the amorphous silicon 42 is coated on a coating 44 of silicon dioxide on a silicon wafer 46. The amorphous silicon 42 is converted to doped polycrystalline silicon by either of two general techniques: (1) a dopant a gaseously diffused into the amorphous coating at an elevated temperature of about 1000°C ; (2) a dopant is ion-implanted into the amorphous coating, and then the coating is heated to about 900°C , this latter technique being preferable because of the lower crystallizing temperature employed. The heating process renders the amorphous silicon polycrystalline whilst the dopant renders it electrically conductive.

What results from the practice of the present invention is a uniform extremely thin transparent electrode coating 48 of polysilicon which may be etched, as is known, into appropriate electrodes . . . and which, most importantly, may be repeated from batch to batch.

The method of the present invention has been found to consistently produce extremely thin polysilicon coatings, for example approximately 100 angstroms, whose uniformity is within ± 20 angstroms of the target thickness.

WHAT WE CLAIM IS:—

1. A method of forming a polysilicon coating on a semiconductor device, said method comprising the steps of evaporating monocrystalline silicon in a vacuum chamber, exposing the semiconductor device to the silicon vapour, thereby depositing amorphous silicon on the semiconductor device, and heating the semiconductor device to a temperature sufficient to crystallize said amorphous silicon.

2. A method according to Claim 1 comprising the step of impregnating said amorphous silicon with impurity atoms.

3. A method according to Claim 2 wherein said amorphous silicon is impregnated with impurities by ion implantation into said amorphous silicon and said amorphous silicon is crystallized by heat at a temperature of approximately 900°C .

4. A method according to Claim 2 wherein an impurity dopant is gaseously diffused into said amorphous silicon at a temperature of approximately 1000°C .



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What results from the practice of the present invention is a uniform extremely thin transparent electrode coating 48 of polysilicon which may be etched, as is known, into appropriate electrodes . . . and which, most importantly, may be repeated from batch to batch.

The method of the present invention has been found to consistently produce extremely thin polysilicon coatings, for example approximately 100 angstroms, whose uniformity is within ± 20 angstroms of the target thickness.

WHAT WE CLAIM IS:—

1. A method of forming a polysilicon coating on a semiconductor device, said method comprising the steps of evaporating monocrystalline silicon in a vacuum chamber, exposing the semiconductor device to the silicon vapour, thereby depositing amorphous silicon on the semiconductor device, and heating the semiconductor device to a temperature sufficient to crystallize said amorphous silicon.

2. A method according to Claim 1 comprising the step of impregnating said amorphous silicon with impurity atoms.

3. A method according to Claim 2 wherein said amorphous silicon is impregnated with impurities by ion implantation into said amorphous silicon and said amorphous silicon is crystallized by heat at a temperature of approximately 900°C .

4. A method according to Claim 2 wherein an impurity dopant is gaseously diffused into said amorphous silicon at a temperature of approximately 1000°C .

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5. A method according to any one of the preceding Claims comprising the steps of monitoring the thickness of said amorphous silicon and terminating said deposition when said amorphous silicon reaches a predetermined thickness.
6. A method according to claim 1 substantially as hereinbefore described with reference to the accompanying drawings.
- 10 7. A semiconductor device formed by the method according to any one of the preceding Claims.
8. A semiconductor device according to Claim 7 substantially as hereinbefore described with reference to, and as shown in, the accompanying drawings.
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