DESCRIPTION

CIRCUIT MEMBER, MANUFACTURING METHOD FOR CIRCUIT MEMBERS, SEMICONDUCTOR DEVICE, AND SURFACE LAMINATION STRUCTURE FOR CIRCUIT MEMBER

TECHNICAL FIELD

[0001]

The present invention is addressed among others to a lamination structure for circuit member surfaces, and a surface treating technique for a lead frame as a circuit member, as well as a semiconductor device using the circuit member, and particularly, to a technique for enhancement of strength in adhesion between a lead frame and a sealing resin in accordance with a type of semiconductor package.

BACKGROUND ART

[0002]

The semiconductor device may be a semiconductor package with a structure having a semiconductor chip, such as an IC chip or LSI chip, mounted on a lead frame, and sealed with an insulating resin. For such semiconductor devices, along with advancements in high-integration and miniaturization, their package structures have developed through such types that had an external lead projecting out of a lateral wall of a resin package, as in an SOJ (small outline J-leaded package) and a QFP (quad flat package), to such types that have an external lead buried for exposure at the backside of a resin package, without projecting outside, and are thin and need a small implementation area, as in a QFN (quad flat non-leaded package) and an SON (small outline non-leaded package).

[0003]

As lead frames, there are known those (e.g. Japanese Patent Application Laying-Open Publication No. 11-40720 (page 4, Fig. 1): patent material-1) having a structure in which, for a frame substrate to be sealed with an insulating

resin, its surfaces are treated for a roughing, and a nickel (Ni) layer and a palladium (Pd) layer are laminated in this order on the surfaces by a plating method. As a method for the roughing process, substrate surfaces of lead frame are chemically polished by an etching solution of an organic acid system.

[0004]

As other known lead frames, there are those (e.g. Japanese Patent Application Laying-Open Publication No. 2004-349497 (page 7, Fig. 3): patent material-2) in which frame substrate surfaces are covered with a plated Ni skin roughed at the obverse side. Formation of such a roughed Ni skin is allowed by adjusting a condition of the plating method.

[0005]

Such being the case, the combination of formation of a plated Ni skin over the surface of a lead frame and provision of Pd or Au plated thereon has a wide use for manufacturing processes to be simplified, and environment-oriented processes to be free of Pb.

[0006]

Further, as circuit members to be brought into close contact with an insulating resin, among others besides lead frames, there are e.g. conductor plates or bus bars of connectors employable in an electrical connection box for distribution of a vehicular power supply to vehicle-mounted auxiliary equipment.

DISCLOSURE OF INVENTION

[0007]

However, the etching solution of organic acid system in the above-noted patent material-1 is effective to a copper surface formed by a plating method, but is little effective for roughing surfaces of a rolled copper plate that is a substrate of lead frame, as a problem. In fact, when treated with such an etching solution of organic acid system, the surface of rolled copper substrate has a raised surface roughness, with a surface profile failing to be needle-shaped. Hence, for lead frames treated for roughing with an etching solution of organic acid system, it was difficult to expect a

great effect with respect to the adhesion to an insulating resin constituting a package. In addition, the surface roughing with an etching solution of organic acid system needs an etching to a 3-μm depth from the copper surface to give a surface roughness (Ra) of 0. 15 μm, and has to make the deeper etching for a greater surface roughness. Such a treating method thus takes time for etching, and has not been adaptive for production a practical lead frame.

[0008]

The above-noted patent material-2 describes a plating method, by which a surface-roughed Ni skin may be formed, but in such a method, the Ni skin needs to be thick to raise the surface roughness, which should be 1 μm or more to provide a stable effect. However, recent trends demand a thin metallic skin, and a Ni skin thickness about 5μm is desirable.

[0009]

By the way, in lead frames applied to semiconductor devices of such a type that is thin and small of implementation area, like QFN or SON, a downside surface of an external lead is exposed at the downside of a resin package, with a resultant small contact area between the external lead and an insulating resin. It therefore is necessary to provide the more enhanced adhesion strength between lead frame and insulating resin. Recent years have observed an increased demand for semiconductor devices addressed to vehicle-mounting, while such applications undergo vibrations as well as temperature variations, needing a greater adhesion strength between lead frame and insulating resin than ever.

[0010]

Further, lead frames are desired to have a matching function to the package type, taking into consideration, among others, those regions of internal leads to be wire-bonded, and those regions of external leads to be soldered to a board for implementation (printed wiring board).

[0011]

It therefore is a main object of the present invention to provide a lead frame allowing for enhancement of adhesion strength to a sealing resin, and a manufacturing

method of the same, as well as a semiconductor device.

[0012]

It is another object of the present invention to provide a lead frame applicable to a package type such as QFN or SON, and a manufacturing method of the same, as well as a semiconductor device.

[0013]

It is still another object of the present invention to provide a surface lamination structure for a circuit member allowing for enhancement of adhesion strength to a sealing resin.

[0014]

According to a first aspect of the present invention, a circuit member includes a frame substrate formed, by patterning a rolled copper plate or a rolled copper alloy plate, with a die pad portion having a surface for a semiconductor chip to be mounted thereon, and a lead portion for an electrical connection to the semiconductor chip, comprising rough surfaces formed on upsides and lateral wall sides of the die pad portion and the lead portion, and the die pad portion and the lead portion having downside surfaces as smooth surfaces, and being configured to be buried in a sealing resin, having a downside of the lead portion exposed.

[0015]

According to a second aspect of the present invention, a circuit member includes a frame substrate formed, by patterning a rolled copper plate or a rolled copper alloy plate, with a die pad portion with a surface for a semiconductor chip to be mounted thereon, and a lead portion for an electrical connection to the semiconductor chip, comprising smooth surfaces as a portion of an upside of the die pad portion and a portion of an upside of the lead portion to be connected to a bonding wire, metallic skins laminated on the smooth surfaces, and rough surfaces formed on regions excepting downsides of the die pad portion and the lead portion and regions where the metallic skins are formed.

[0016]

Further, those portions of the circuit member to be brought into contact with

a resin sealing mold may comprise smooth surfaces.

[0017]

It is noted that in the present invention, the above-noted rough surfaces may preferably have a surface roughness (Ra) of 0.3 μm or more, and a laminated metallic skin may preferably comprise a Ni skin of a thickness within a range of 0.5 to 2 μm, a Pd skin of a thickness within a range of 0.005 to 0.2 μm, and an Au skin of a thickness within a range of 0.003 to 0.01 μm, as they are laminated in order. The above-noted rough surfaces may preferably be formed by treating by a micro-etching solution having hydrogen peroxide and sulfuric acid as components. Here, the micro-etching solution refers to a surface treating agent adapted for a slight dissolving of a metal surface to form a rough surface comprising minute undulations.

[0018]

According to a third aspect of the present invention, a manufacturing method for circuit members comprises the steps of forming a frame substrate with a die pad portion and a lead portion, by patterning a rolled copper plate or a rolled copper alloy plate, roughing upside surfaces and lateral wall surfaces of the frame substrate, using a micro-etching solution having hydrogen peroxide and sulfuric acid as components, with a making material covering downside surfaces of the frame substrate, and having, past a removal of the masking material, metallic skins laminated on obverse surfaces of the frame substrate.

[0019]

According to a fourth aspect of the present invention, a manufacturing method for circuit members comprises the steps of forming a frame substrate with a die pad portion and a lead portion, by patterning a rolled copper plate or a rolled copper alloy plate, laminating metallic skins on an upside surface of the die pad portion, and on a portion of the lead portion to be connected to a bonding wire, processing by surface-roughing the frame substrate, using a micro-etching solution having hydrogen peroxide and sulfuric acid as principal components, with a masking material covering downside surfaces of the frame substrate, and removing the masking material.

[0020]

The metallic skins laminated on the upside surface of the die pad portion and on the portion of the lead portion to be connected to the bonding wire may preferably each comprise an Ag skin within a range of 2 to 15 μm, or a metallic skin having a Ni skin and a Pd skin laminated in order on the frame substrate.

[0021]

According to a fifth aspect of the present invention, a semiconductor device comprises a circuit member composed of a rolled copper plate or a rolled copper alloy plate, comprising a die pad portion and a lead portion, rough surfaces formed on upsides and lateral wall sides of the die pad portion and the lead portion, smooth surfaces as downside surfaces of the die pad portion and the lead portion, and metallic skins formed on the surfaces, a semiconductor chip mounted on an upside of the die pad portion, a bonding wire interconnecting the semiconductor chip and the lead portion, and an electrically insulating sealing resin configured to have the circuit member, the semiconductor chip, and the bonding wire sealed in, with a downside of the lead portion exposed.

[0022]

According to a sixth aspect of the present invention, a semiconductor device comprises a circuit member composed of a rolled copper plate or a rolled copper alloy plate, comprising a die pad portion and a lead portion, smooth surfaces as an upside surface of the die pad portion and a portion of an obverse side surface of the lead portion to be connected to a bonding wire, metallic skins laminated on the smooth surfaces, and rough surfaces formed on regions excepting reverse sides of the die pad portion and the lead portion and regions where the metallic skins are formed, a semiconductor chip mounted on the upside of the die pad portion, the bonding wire interconnecting the semiconductor chip and the lead portion, and an electrically insulating sealing resin configured to have the circuit member, the semiconductor chip, and the bonding wire sealed in, with a downside of the lead portion exposed.

[0023]

According to a seventh aspect of the present invention, a surface lamination

structure for a circuit member to be joined to an insulating resin comprises a rough surface formed on an obverse side of a conductive substrate composed of a rolled copper plate or a rolled copper alloy, with a surface roughness (Ra) of 0.3 μm or more, and a Ni skin and a Pd skin laminated in order on the rough surface, wherein the Ni skin has a thickness within a range of 0.5 to 2 μm, and the Pd skin has a thickness within a range of 0.005 to 0.2 μm.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024]

Fig. 1 is a plan view of a lead frame according to a first embodiment of the present invention.

Fig. 2 is a sectional view illustrating a process of a manufacturing method of the lead frame according to the first embodiment of the present invention.

Fig. 3 is a sectional view illustrating a process of the manufacturing method of the lead frame according to the first embodiment of the present invention.

Fig. 4 is a sectional view illustrating a process of the manufacturing method of the lead frame according to the first embodiment of the present invention.

Fig. 5 is a sectional view illustrating a process of the manufacturing method of the lead frame according to the first embodiment of the present invention.

Fig. 6 is a sectional view illustrating a process of the manufacturing method of the lead frame according to the first embodiment of the present invention.

Fig. 7 is a sectional view illustrating a process of a manufacturing method of a semiconductor device according to the first embodiment of the present invention.

Fig. 8 is a sectional view illustrating a process of the manufacturing method of the semiconductor device according to the first embodiment of the present invention.

Fig. 9 is a sectional view of the semiconductor device according to the first embodiment of the present invention.

Fig. 10 is an enlarged sectional view of a roughed portion of a lead frame according to an embodiment of the present invention.

Fig. 11 is a perspective view illustrating an outline of an adhesion strength test.

Figs. 12(a) to (d) are sectional views illustrating a sequence of manufacturing processes of a lead frame according to a second embodiment of the present invention.

Figs. 13(a) to (d) are sectional views illustrating a sequence of manufacturing processes of a semiconductor device according to the second embodiment of the present invention.

Fig. 14 is an enlarged sectional view of a roughed portion of a lead frame according to another embodiment of the present invention.

Figs. 15(a) to (e) are sectional views illustrating a sequence of manufacturing processes of a lead frame according to a third embodiment of the present invention.

Figs. 16(a) to (e) are sectional views illustrating a sequence of manufacturing processes of a semiconductor device according to the third embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0025]

There will be detailed circuit members, manufacturing methods for circuit members, semiconductor devices, and surface lamination structures for circuit members according to embodiments of the present invention, with reference to the drawings. It is now noted that the drawings are schematic, and for respective material layers, the thickness, its ratio, etc. are different from practical ones. Specific thickness and dimensions should thus be decided in consideration of the following description. Further, drawings may involve also such parts as mutually different in between in dimensional relationship or ratio, as a matter of course.

[0026]

[First Embodiment]

Fig. 1 to Fig. 9 show a first embodiment of the present invention. Fig. 1 is a

plan view of a lead frame, and Fig. 2 to Fig. 9 illustrate processes in a manufacturing method of the lead frame, as well as of a semiconductor device, with respect to a section A-A of Fig. 1.

[0027]

(Configuration of lead frame)

According to the present embodiment, a lead frame 1 is manufactured in the form of a frame substrate 2 as a rolled copper plate or rolled copper alloy plate of an elongate ribbon shape that is patterned by, among others, an etching or a die-blanking, to have a plurality of consecutive unit patterns. It is noted that Fig. 1 shows a single unit pattern in the lead frame 1.

[0028]

As shown in Fig. 1, the unit pattern of lead frame 1 has a die pad portion 3 formed, in a central region, in a rectangular shape for a semiconductor chip to be mounted thereon, a set of lead portions 8 formed so as to surround the die pad portion 3, a set of tie bars 6 linking the die pad portion 3 with the frame substrate 2, and a set of tie bars 7 laterally interlinking lead portions 8. Those lead portions 8 are set in such sizes that will not project out of a lateral wall of a sealing resin 15, as will be described. It is noted that this embodiment, which is formed with tie bars 7 laterally interlinking lead portions 8, may be modified by omission of tie bars 7, to such a pattern that has lead portions 8 extending from an outer frame part of the frame 2 toward a periphery of the die pad portion 3.

[0029]

For the lead frame 1 according to the present embodiment, upside surfaces (surfaces at that side on which a semiconductor chip is to be mounted) as well as lateral wall surfaces are treated for a roughing by using a micro-etching solution including hydrogen peroxide and sulfuric acid as principal components, to provide rough surfaces 3A and 3B as well as 8A and 8B, as shown in Fig. 4 and Fig. 5. For these rough surfaces 3A, 3B and 8A, 8B, the surface roughness (Ra) is set within a range of 0.3 μm or more, and their surface profiles are undulated with needle-shaped projections. The frame substrate 2 has downside surfaces (surfaces at the opposite side

to the semiconductor chip mounting side) formed as smooth surfaces.

[0030]

Further, as shown in Fig. 6, metallic skins 10 are plated on surfaces of the frame substrate 2 including die pad portions 3, lead portions 8, etc. It is noted that in this embodiment, as shown in Fig. 10, each metallic skin 10 is composed of a Ni skin 17 and a Pd skin 18 laminated in this order on surfaces of the frame substrate 2. And the thickness is set within a range of 0.5 to 2 μm for the Ni skin 17, and within a range of 0.0055 to 0.2 μm for the Pd skin 18. It also is noted that the Pd skin 18 is a metallic layer having a good property for connections to a bonding wire and solder paste, allowing for integrities in, among others, a wire bonding for connection of a bonding wire 13 shown in Fig. 7, and a soldering to an unshown board for implementation (a printed wiring board).

[0031]

In such the configuration of lead frame 1, for rough surfaces 3A, 3B and 8A, 8B, the surface roughness (Ra) is set within a range of 0.3 μm or more, and ranges of thickness are set for Ni skin 17 and Pd skin 18 constituting each metallic skin 10, thereby allowing a secured configuration of needle-shaped projections of surfaces coated with metallic skins 10, without breaking surface profiles of rough surfaces 3A, 3B and 8A, 8B. Therefore, when the lead frame 1 is sealed with a resin, minute projections involving metallic skin 10 may exhibit anchoring effects to bite in the sealing resin.

[0032]

(Manufacturing method of lead frame)

Description is now made of a manufacturing method of a lead frame according to the present embodiment, with reference to Fig. 2 to Fig. 6.

[0033]

In this embodiment, there is first provided a frame substrate 2 formed with die pad portions 3, lead portions 8, etc., as shown in Fig. 2. For the frame substrate 2 (a rolled copper alloy plate), the constituent material to be employed may be, e.g., a Mitsubishi Metex make, low-tin, Ni-copper alloy MF202.

[0034]

Next, as shown in Fig. 3, the frame substrate 2 has a protecting film 9 laminated as a masking material on a downside (one principal plane) thereof. Then, those portions of the frame substrate 2 not covered by the protecting film 9 are micro-etched for approximately 90 seconds, by dipping in a micro-etching solution including hydrogen peroxide and sulfuric acid as principal components, to form such rough surfaces 3A, 3B and 8A, 8B as shown in Fig. 4. These rough surfaces 3A, 3B and 8A, 8B have surface profiles undulated like precipitous needles. Such a roughing treatment resulted in an etching magnitude of 2 μm, a surface roughness (Ra) of 0.33 μm, and an S(-)ratio of 2.08 on rough surfaces 3A, 3B and 8A, 8B. It is noted that the etching magnitude means an average digging depth of etching. The Sratio represents a value of a surface area of undulating surface divided by an area of flat plane in a measured range.

[0035]

Thereafter, as shown in Fig. 5, the protecting (masking material) film 9 is separated, and such metallic skins 10 as shown in Fig. 6 are formed. It is noted that the metallic skins 10 are each composed of a Ni skin 17 and a Pd skin 18 laminated in this order on surfaces of the frame substrate 2, as described. It also is noted that the method to be employed for formation of metallic skin 10 may be a well-known method, such as an electrolytic plating or electroless plating. Here, the growth of metallic skin is controlled so that the Ni skin 17 has a thickness within a range of 0.5 to 2 μm, and the Pd skin 18 has a thickness within a range of 0.005 to 0.2 μm. Like this, manufacture of a lead frame is completed.

[0036]

According to the present embodiment, the manufacturing method of lead frame can have a shorter etching time, and an enhanced productivity. Further, thin metallic skins 10 allow for a reduced consumption of an expensive plating solution.

[0037]

Description is now made of a manufacturing method of a semiconductor

device, as well as configuration of the semiconductor device, with reference to Fig. 7 to Fig. 9.

[0038]

As shown in Fig. 7, a semiconductor chip 11 is mounted, via a paste agent 12, on an upside surface of a die pad portion of a lead frame 1 manufactured by the above-noted manufacturing method. Thereafter, by way of a wire bonding, lead portions 8 are connected, by bonding wires 13, at their distal ends to corresponding electrodes of the semiconductor chip 11. Next, as shown in Fig. 8, the lead frame 1 has a resin leak preventing protection film 14 laminated on a downside thereof, and the entirety is molded with a sealing resin 15 made of, e.g., an epoxy resin. Thereafter, the combination of sealing resin 15 and lead frame 1 is cut (diced) in a desirable form, whereby such a semiconductor device (semiconductor package) 16 as shown in Fig. 9 is finished up.

[0039]

In the semiconductor device 16 of this embodiment, downside surfaces of die pad portion 3 and lead portions 8 are exposed at a downside of the sealing resin 15. Exposed lead portions 8 are to be each connected by a soldering to an end of an unshown board for implementation (a printed wiring board).

[0040]

For such the configuration of semiconductor device 16 in which obverse surfaces of die pad portion 3 and lead portions 8 are roughed, excepting downside surfaces, their adhesion strength to the sealing resin 15 is high, affording a durability against vibrations and temperature variations.

[0041]

Description is now made of a comparison between a case of a roughing treatment to a rolled copper alloy plate according to the present embodiment, and a case of treatment in an organic acid system.

[0042]

Compared in Table-1 below are combinations of etching magnitude, surface roughness (Ra), Sratio, and etching time in an example of surface treatment using a

micro-etching solution including hydrogen peroxide and sulfuric acid as principal components in accordance with the present embodiment, and in comparative examples using an organic acid system (where CZ8100 ® is employed) as in the past. Comparative examples are enumerated for etching magnitudes of 1 μm, 2 μm, and 3 μm.

(Table-1)

Treating solution	Hydrogen peroxide + sulfuric acid	Comparative examples by organic acid system (C28100)		
Etching magnitude	2 μm	1 μm	2 μm	3 μm
Roughness (Ra)	0.33 μm	0.085 μm	0.105 μm	0.152 μm
Sratio	2.08	1.11	1.13	1.20
Etching time	approx. 1.5 min	approx. 3 min	approx. 6 min	approx. 9 min

[0043]

It will be seen from comparative examples in the Table-1 above that the use of organic acid system needs an etching of 3 μm depth to obtain a roughness of 0.15 μm. As will be seen therefrom, it is necessary for a greater roughness to make a deeper etching, taking time for the etching, with a resultant non-conformity to production of a practical lead frame. To the contrary, in a surface treatment according to the present embodiment, it is possible to obtain a roughness of comparative example times two or more by an etching depth of 2 μm. In the present embodiment, the surface treatment is effected by using a micro-etching solution including hydrogen peroxide and sulfuric acid as principal components, allowing for provision of a surface configuration with minute needle-shaped undulations. This configuration is considered effective to achieve a greater anchoring effect than would be supposed from a numerical representation of parameter.

[0044]

For a measurement of adhesion strength to a sealing resin in the present embodiment, such a cup shearing strength as shown in Fig. 11 was measured. On a rolled copper alloy plate of a copper alloy (MF202), a metallic skin like the above-noted was formed, and a discoloration preventing process was provided, whereby an adhesion strength test piece 20 was made. This adhesion strength test piece 20 was heated once at 220 °C for 60 seconds on a hot plate, and thereafter, additionally, at 220 °C for 60 seconds on the hot plate, and further, at 240 °C for 80 seconds on the hot plate. For the molding, a heating under a pressure of 125 kg/cm^2 was performed at 175 °C for 120 seconds. Thereafter, an additional heating was performed at 175 °C for 5 hours, whereby an epoxy resin 21 was hardened.

[0045]

On thus molded epoxy resin 21 and adhesion strength test piece 20, a load was imposed in a direction of arrows shown in Fig. 11, and the load when they were separated was divided by the area of joint surface, to determine a load (kN/cm^2) per unit area.

[0046]

As a result of this, the following values were given as values of shearing strength, proving that a roughing process according to the present embodiment had an enhancing effect on the adhesion strength to sealing resin.

[0047]

(1) 0.04 kN/cm^2 for no roughing

(2) 0.42 kN/cm^2 for a roughing without anti-corrosion process

(3) 0.54 kN/cm^2 for a roughing with a silane series anti-corrosion process

[Second Embodiment]

Description is now made of a second embodiment of the present invention, with reference to Fig. 12 and Fig. 13. It is noted that in this embodiment, like parts to the first embodiment are designated by like reference characters, for elimination of redundancy.

[0048]

According to the second embodiment, for a lead frame as a circuit member, those surface portions to be brought into contact with a resin sealing mold are made smooth, and the remaining surface portions are roughed, to effect prevention of resin leakage and occurrences of resin burrs when molding the sealing resin. Fig. 12(a) shows a section of a frame substrate 2 patterned like Fig. 2. For the partial roughing, as shown in Fig. 12(b), instead of the method of laminating a protecting film on a downside of a frame substrate 2 described with reference to Fig. 3, there is employed a method of pinching a frame substrate 2 by a pair of upper and lower etching jigs 29 and 30, with rubber packing elements 27 and 28 put in between, and injecting a micro-etching solution 32 from a nozzle 31 provided through the etching jig 29, for a prescribed period of time, onto the frame substrate 2 to be micro-etched for surface roughing.

[0049]

In this occasion, the rubber packing element 27, which covers a downside of the frame substrate 2, and the rubber packing element 28, which covers those surface portions of an upside of the frame substrate 2 to be brought into contact with the resin sealing mold, serve as masking materials for protection against micro-etching of those surface portions of the frame substrate 2 to be left smooth.

[0050]

Fig. 12 (c) shows the frame substrate 2 in a condition after the etching, where it is taken out of the etching jigs, and those portions 24 of downside surfaces 23 and upside surfaces having been covered by the rubber packing element 27 (i.e. the surface portions to be brought into contact with the resin sealing mold) are left as smooth surfaces, and the remaining surfaces are formed as rough surfaces 3A, 3B and 8A, 8B.

[0051]

Next, as shown in Fig. 12(d), metallic skins 10 are plated on surfaces of the frame substrate 2 including a die pad portion 3 and lead portions 8, like the first embodiment.

[0052]

Fig. 13 shows a sequence of processes using such a lead frame 1A for manufacture of a semiconductor device. For the lead frame 1A, as shown in Fig. 13(a), a semiconductor chip 11 is mounted on an upside of a die pad portion, with a paste agent 12 in between, and then, by way of a wire bonding, lead portions 8 are connected by bonding wires 13 to corresponding electrodes of the semiconductor chip 11.

[0053]

Next, as shown in Fig. 13(b), using a resin sealing mold 25, they are molded with a sealing resin 15. Fig. 13(c) shows a condition after the resin molding, where the lead frame is taken out of the resin sealing mold 25. Under this condition, unnecessary parts of lead portions are cut in a desirable form, whereby the semiconductor (semiconductor package) is finished up, as in Fig. 13(d). It is noted that this embodiment provides an illustrative example of individual molding, involving no dicer cutting processes for a dicing such as in a lump molding.

[0054]

In the resin molding by the sealing resin in Fig. 13(b), if those surface portions of the lead frame 1A contacting the resin sealing mold 25 were rough, the resin sealing mold 25 and the lead frame 1A might have had gaps in between, where sealing resin might have intruded, forming burrs, or sealing resin might have leaked outside the mold in an extreme case. In the present embodiment in which also roughed surface portions do provide like effects to the first embodiment, those surface portions of the lead frame 1A to be brought into contact with the resin sealing mold 25 are formed as smooth surfaces, and the resin sealing mold 25 is in close contact with the lead frame 1A, with an effect to prevent resin burrs or resin leakage.

[0055]

[Third Embodiment]

Description is now made of a circuit member according to a third embodiment of the present invention, with reference to Fig. 15 and Fig. 16. It is noted that in this embodiment, like parts to the first embodiment are designated by like

reference characters, for elimination of redundancy.

[0056]

This embodiment provides in advance a frame substrate 2 shown in Fig. 15(a), which is made of a rolled copper alloy, and has a prescribed pattern of lead frame formed thereon, including a die pad portion 3, lead portions 8, etc., by an etching or die-blanking.

[0057]

Next, as shown in Fig. 15(b), precious-metal skins 10B are plated on a semiconductor chip mounting portion of a die pad upside surface and on bonding wire connecting portions of lead upside surfaces of the frame substrate 2, and as shown in Fig. 15(c), a protecting (masking material) film 9 is laminated on a downside of the frame substrate 2.

[0058]

Next, a micro-etching solution is injected over surfaces of the frame substrate 2, or the frame substrate 2 is dipped in a micro-etching solution for a prescribed time period (approximately 90 seconds), for a micro-etching to form such roughed surfaces 3A, 3B and 8A, 8B as shown in Fig. 15(d). In this state, those portions of surfaces of the frame substrate 2 where precious-metal skins 10B are plated, and those portions where the protecting film 9 is laminated are kept from the micro-etching, so that there are left surfaces of the frame substrate 2 per se, as they are smooth. Fig. 15(e) is a section of the lead frame 1, as it is past a removal of the protecting film 9, and is finished up, where precious-metal skins 10B have their smooth surfaces left as they are, as well as downside surfaces 23, and other surfaces else than those are formed as rough surfaces 3A, 3B and 8A, 8B.

[0059]

It is now noted that the precious-metal skins 10B are each composed of an Ag skin, or of an Ni skin and a Pd skin laminated in this order on a surface of the frame substrate 2.

[0060]

Fig. 16 shows a sequence of processes for manufacturing a QFN (quad

flat non-leaded package) using a lead frame manufactured by processes in Fig. 15 in accordance with the present invention. Fig. 16(a) shows a section of the lead frame having a multiplicity of unit patterns formed thereon corresponding to Fig. 15(e).

[0061]

Next, as shown in Fig. 16(b), a resin burr preventing film is affixed to a downside of the lead frame, as necessary, and a semiconductor chip 11 is mounted on an upside of a die pad portion, with a paste agent 12 in between, and thereafter, by way of a wire bonding, lead portions 8 are connected by bonding wires 13 to corresponding electrodes of the semiconductor chip 11.

[0062]

Next, as shown in Fig. 16(c), using a resin sealing mold (lump-molding mold) 25, they are lump-molded (resin-sealed) with a sealing resin 15.

[0063]

Next, for an enhanced solder connectability in implementation, as shown in Fig. 16(d), solder skins 22 are plated on die pad portion and lead portions exposed in part outside the sealing resin, and then, the lump-molded lead frame is dicer-cut along dicing cut ways 26, whereby as shown in Fig. 16(e), an individual semiconductor device is finished up.

[0064]

The third embodiment also exhibits like effects to the first embodiment. It is noted that in this embodiment, metallic skins are plated simply on a semiconductor chip mounting surface as well as on wire bonding surfaces, and a downside of each lead portion to be soldered has a solder skin plated thereon, thus allowing for a saving of an expensive precious-metal plating solution, a controlled low production cost, and an enhanced wire bondability as well as mountability of secmiconductor chip 11.

[0065]

[Surface Lamination Structure for Circuit Members]

Description is now made of a surface lamination structure for circuit members according to the present invention, with reference to Fig. 10. On an obverse

side of a frame substrate 2 as a conductive material composed of a rolled copper plate or a rolled copper alloy plate, there is a rough surface 8A formed with a roughness of 0.3 μm or more, where a Ni skin 17 and a Pd skin 18 are laminated in this order. Preferably, the thickness of Ni skin should range 0.5 to 2 μm, and that of Pd skin, 0.005 to 0.2 μm. Such a surface lamination structure affords an enhanced adhesion strength between conductive material and insulating resin. Further, as shown in Fig. 14, there may be an Au skin 19 plated for lamination on the Pd skin 18, with a thickness within a range of 0.003 to 0.01 μm. Such the Au skin is effective to prevent an oxide film from being formed on the Pd skin.

[0066]

[Other Embodiments]

Such drawings and description as part of disclosure of the foregoing embodiments should not be construed restrictive to the present invention. For artisan, varieties of substitute modes of embodiment, embodiment examples, and techniques for implementation will become apparent from such disclosure.

[0067]

For example, the first, second, and third embodiment, in which the metallic skin 10 is formed as a lamination of a single layer of Ag skin, or double layers of Ni skin 17 and Pd skin 18, may be modified to have a metallic skin 10A formed as a lamination with an additional Au skin 19 plated on the Pd skin 18, as in the surface lamination structure for circuit members shown in Fig. 14. It is noted that, preferably, the Au skin 19 should have a thickness within a range of 0.003 to 0.01 μm.

[0068]

The foregoing first, second, and third embodiment, which are addressed to package types thin and small of implementation area, such as QFN and SON, may well be addressed to such types of lead frames as SOP and FLGA, allowing for an enhanced adhesion strength to sealing resin.

[0069]

Further, the foregoing first, second, and third embodiment, in which a lead

frame is applied for description of a circuit member, may be addressed to such circuit members as conductor plates or bus bars of connectors employable in an electrical connection box for distribution of a vehicular power supply to vehicle-mounted auxiliary equipment.

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CLAIMS:

1. A circuit member including a frame substrate formed, by patterning a rolled copper plate or a rolled copper alloy plate, with a die pad portion for a semiconductor chip to be mounted thereon, and a lead portion for an electrical connection to the semiconductor chip, comprising:

rough surfaces formed as roughed surfaces on upsides and lateral wall sides of the die pad portion and the lead portion; and

smooth surfaces formed on downsides of the die pad portion and the lead portion, wherein

the die pad portion and the lead portion are configured to be buried in a sealing resin, having a downside of the lead portion exposed.

2. The circuit member as claimed in claim 1, comprising metallic skins formed on obverse surfaces of the die pad portion and the lead portion, for enhancement of connectability with a bonding wire and a solder paste.

3. A circuit member including a frame substrate formed, by patterning a rolled copper plate or a rolled copper alloy plate, with a die pad portion for a semiconductor chip to be mounted thereon, and a lead portion for an electrical connection to the semiconductor chip, comprising:

smooth surfaces formed on a portion of an upside of the die pad portion and on a portion of an upside of the lead portion to be connected to a bonding wire;

metallic skins on the smooth surfaces; and

rough surfaces formed on regions excepting downsides of the die pad portion and the lead portion and regions where the metallic skins are formed.

4. The circuit member as claimed in claim 3, wherein a metallic skin comprises an Ag skin.

5. The circuit member as claimed in claim 3, wherein a metallic skin comprises a Ni skin and a Pd skin laminated in order on the rolled copper plate.

6. The circuit member as claimed in claim 3, wherein a metallic skin comprises a Ni skin, a Pd skin, and an Au skin laminated in order on the rolled copper

plate.

7. The circuit member as claimed in claim 3, wherein a rough surface has a surface roughness (Ra) of 0.3 μm or more.

8. The circuit member as claimed in claim 4, wherein the Ag skin has a thickness within a range of 2 to 15 μm.

9. The circuit member as claimed in claim 5, wherein the Ni skin has a thickness within a range of 0.5 to 2 μm, and the Pd skin has a thickness within a range of 0.005 to 0.2 μm.

10. The circuit member as claimed in claim 6, wherein the Ni skin has a thickness within a range of 0.5 to 2 μm, the Pd skin has a thickness within a range of 0.005 to 0.2 μm, and the Au skin has a thickness within a range of 0.003 to 0.01 μm.

11. The circuit member as claimed in claim 1, wherein a rough surface is treated by a micro-etching solution having hydrogen peroxide and sulfuric acid as components.

12. A manufacturing method for circuit members, comprising:

forming a frame substrate with a die pad portion and a lead portion, by patterning a rolled copper plate or a rolled copper alloy plate;

roughing upside surfaces and lateral wall surfaces of the frame substrate, using a micro-etching solution having hydrogen peroxide and sulfuric acid as components, with a making material covering downside surfaces of the frame substrate; and

having, past a removal of the masking material, metallic skins laminated on obverse surfaces of the frame substrate.

13. A manufacturing method for circuit members, comprising:

forming a frame substrate with a die pad portion and a lead portion, by patterning a rolled copper plate or a rolled copper alloy plate;

laminating metallic skins on an upside surface of the die pad portion, and on a portion of the lead portion to be connected to a bonding wire;

surface-roughing the frame substrate, using a micro-etching solution having hydrogen peroxide and sulfuric acid as principal components, with a masking

material covering downside surfaces of the frame substrate having the metallic skins laminated thereon; and

removing the masking material.

14. The manufacturing method for circuit members as claimed in claim 12, wherein the step of laminating the metallic skins comprises laminating an Ag skin on an obverse surface of the frame substrate.

15. The manufacturing method for circuit members as claimed in claim 12, wherein the step of laminating the metallic skins comprises laminating a Ni skin and a Pd skin in order on an obverse surface of the frame substrate.

16. The manufacturing method for circuit members as claimed in claim 15, comprising laminating an Au skin on the Pd skin.

17. A semiconductor device comprising:

a circuit member composed of a rolled copper plate or a rolled copper alloy plate, comprising:

a die pad portion and a lead portion;

rough surfaces formed on upsides and lateral wall sides of the die pad portion and the lead portion;

smooth surfaces formed on downsides of the die pad portion and the lead portion; and

metallic skins on the surfaces;

a semiconductor chip mounted on an upside of the die pad portion;

a bonding wire interconnecting the semiconductor chip and the lead portion; and

an electrically insulating sealing resin configured to have the circuit member, the semiconductor chip, and the bonding wire sealed in, with a downside of the lead portion exposed.

18. A semiconductor device comprising:

a circuit member composed of a rolled copper plate or a rolled copper alloy plate, comprising:

a die pad portion and a lead portion;

smooth surfaces formed on an upside of the die pad portion, and on a portion of an obverse side of the lead portion to be connected to a bonding wire;

metallic skins on the smooth surfaces; and

rough surfaces formed on regions excepting reverse sides of the die pad portion and the lead portion and regions where the metallic skins are formed;

a semiconductor chip mounted on the upside of the die pad portion;

the bonding wire interconnecting the semiconductor chip and the lead portion; and

an electrically insulating sealing resin configured to have the circuit member, the semiconductor chip, and the bonding wire sealed in, with a downside of the lead portion exposed.

19. A surface lamination structure for a circuit member to be joined to an insulating resin, comprising:

a rough surface formed on an obverse side of a conductive substrate composed of a rolled copper plate or a rolled copper alloy, with a surface roughness (Ra) of 0.3 μm or more; and

a Ni skin and a Pd skin laminated in order on the rough surface, wherein

the Ni skin has a thickness within a range of 0.5 to 2 μm, and the Pd skin has a thickness within a range of 0.005 to 0.2 μm.

20. The surface lamination structure for a circuit member as claimed in claim 19, further comprising an Au skin laminated on the Pd skin, with a thickness within a range of 0.003 to 0.01 μm.