

MRAM with Eddy Current Barrier

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Technical Field

This invention relates to magnetoresistive random access memory ("MRAM") with an eddy current barrier and refers particularly, though not exclusively, to

5 MRAM with an eddy current barrier to reduce eddy current interference.

Background

A known MRAM structure is schematically shown in Figure 1. On a substrate 101 are: a reference layer 103, an interface layer 105, an insulating layer 107, a

10 second interface layer 109, and a free layer 111. A cap layer 113 is the topmost layer and is opposite the substrate 101. The electric current is shown by arrow 115 and magnetic pinning by arrow 117. Magnetic flipping is bidirectional as shown by arrow 119.

15 With MRAM, as each device is scaled down, the induced magnetic field may overlap with adjacent cells, leading to potentially incorrect writes in the adjacent cell. This problem is sometimes called the half-select or write disturb problem. As such it has been long believed that MRAM is limited to a relatively large cell size. Also, during fast write cycles, eddy current tunneling may result in leakage

20 to an adjacent cell. The problem is mainly in the second interface layer 109, and free layer 111, where external interference, particularly from the pinning layers 103, 105 of an adjacent cell, may cause an incorrect write in the flipping layers 109, 111.



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Furthermore, for some time MRAM has been suggested as having lower switching energy with faster switching speed. However, by placing the individual cells close to each other, magnetic stray field interference can happen due to pin layer magnetic orientation.

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Summary

According to an exemplary aspect there is provided a magnetoresistive random access memory ("MRAM") device comprising a plurality of layers on a substrate. The plurality of layers comprises pinning layers, flipping layers, and at least one
10 insulating layer between the pinning layers and the flipping layers. An eddy current side wall encapsulates at least the pinning layers of the plurality of layers. The eddy current side wall comprises a grain insulating layer for electrical insulation, and a magnetic barrier layer for magnetic isolation.

15 The MRAM device may further comprise a cap layer on the plurality of layers remote from the substrate. The eddy current side wall may extend between the substrate and the cap layer for reducing potential interference both magnetically and electrically. The grain insulating layer may be over the flipping layers, and the magnetic barrier layer may be over the grain insulating layer.

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According to another exemplary aspect there is provided a magnetoresistive random access memory ("MRAM") device comprising a plurality of layers on a substrate. The plurality of layers comprises pinning layers, flipping layers, and at least one insulating layer between the pinning layers and the flipping layers.

A cap layer is over the plurality of layers remote from the substrate. An eddy current side wall encapsulates and insulating the plurality of layers. The eddy current side wall extends from and between the cap layer and the substrate.

- 5 For both aspects the eddy current side wall may extend between an upper surface of the substrate to at least one of a side wall and a lower surface of the cap layer.

According to a further exemplary aspect, there is provided a method of
10 insulating a magnetoresistive random access memory ("MRAM") device. The MRAM device comprises a plurality of layers on a substrate. The plurality of layers comprises pinning layers, flipping layers, and at least one insulating layer between the pinning layers and the flipping layers. The method comprises forming an eddy current side wall encapsulating at least the pinning layers of
15 the plurality of layers. The eddy current barrier is formed by first forming one of a grain insulating layer for electrical insulation and a magnetic barrier layer for magnetic isolation, then forming the other of the grain insulating layer for electrical insulation and the magnetic barrier layer for magnetic isolation.

- 20 For the further aspect, the grain insulating layer for electrical insulation may be formed over side walls of at least the plurality of flipping layers. The magnetic barrier layer may be formed over the grain insulating layer. Before forming the eddy current side wall, a photoresist layer may be formed over those surfaces where the eddy current side wall is not required. The eddy current side wall may

be formed by one of: plating, and sputtering. The method may further comprise forming a cap layer on the plurality of layers remote from the substrate. The eddy current side wall may be formed between the substrate and the cap layer for reducing potential interference both magnetically and electrically. The eddy
5 current side wall may be formed between an upper surface of the substrate to at least one of a side wall and a lower surface of the cap layer.

For all aspects, the magnetic barrier layer may comprise a material having relatively high paramagnetic properties. The material may be selected from:
10 copper, and a compound of copper having a high copper content. The grain insulating layer may comprise: an O_3 compound, or an O_3 compound of a metal. The grain insulating layer may be: Al_2O_3 , Fe_2O_3 or B_2O_3 .

Brief Description of the Drawings

15 In order that the invention may be fully understood and readily put into practical effect there shall now be described by way of non-limitative example only exemplary embodiments, the description being with reference to the accompanying illustrative drawings.

20 In the drawings:

Figure 1 is a schematic illustration of a known, typical MRAM structure;

Figure 2 is a schematic illustration of an exemplary embodiment of an MRAM structure; and

Figure 3 is a schematic illustration of another exemplary embodiment of an MRAM structure.

Detailed Description of the Exemplary Embodiments

- 5 In the drawings like components have like reference numerals with a prefix number indicating the relevant drawing figure.

As mentioned above, a known MRAM structure 100 is schematically shown in Figure 1. On a substrate 101 are: a reference layer 103, an interface layer 105,
10 an insulating layer 107, a second interface layer 109, and a free layer 111. A cap layer 113 is the topmost layer and is opposite the substrate 101107 (as an electrical connection layer). A grain-to-grain insulator (not shown) is provided. The electric current is shown by arrow 115 and magnetic pinning by arrow 117. Magnetic flipping is bidirectional as shown by arrow 119. This structure suffers
15 from the half-select or write disturb problem; eddy current tunneling during fast write cycles; eddy current leakage to an adjacent cell; magnetic stray field interference; and imperfect anisotropy uniformity during thermal conditions.

In Figure 2 there is shown an exemplary embodiment of an MRAM structure
20 200. On a substrate 201 are: a reference layer 203, an interface layer 205, an insulating layer 207, a second interface layer 209, and a free layer 211. A cap layer 213 is the topmost layer and is opposite the substrate 201. The electric current is shown by arrow 215 and magnetic pinning by arrow 217. Magnetic flipping is bidirectional as shown by arrow 219. All of this is similar to the known

structure of Figure 1. In addition, for the exemplary embodiment there is an eddy current side wall generally designated as 221 over the MRAM structure 200.

- 5 The eddy current side wall 221 is not conducive to conducting eddy currents and is also generally electrically insulating. It has two component layers: a grain isolation layer 223 for electrical insulation, and a magnetic barrier layer 224 for magnetic isolation. As shown, the grain isolation layer 223 is immediately adjacent the MRAM structure 200 and the magnetic barrier layer 224 is applied
10 over the grain isolation layer 223. However, the magnetic barrier layer 224 may be immediately adjacent the MRAM structure 200, and the grain isolation layer 223 may be applied over the magnetic barrier layer 224.

The grain isolation layer 223 is of a material that provides electrical current
15 protection preferably by electrically shorting an external interference signal. It may be of any suitable material such as, for example, an O_3 compound, particularly an O_3 compound of a metal. A metal is preferred for rigidity. For example, the grain isolation layer 223 may be one or more of: Al_2O_3 , Fe_2O_3 and B_2O_3 . The grain isolation layer 223 covers at least the flipping layers 209, 211 to
20 shield them from external signals that may cause incorrect writes; and also may stop interference signals emanating from the flipping layers 209, 211. Preferably, the grain isolation layer 223 fully encapsulates the MRAM structure 200 from an upper surface 225 of the substrate 201 to a side wall 227 or lower surface 229 of the cap layer 213.

The grain isolation layer 223 may be applied using known techniques such as, for example, plating or sputtering of AlO or SiO, after applying a photoresist layer to those surfaces not requiring the grain layer 223 (e.g. the top of free layer 211 or cap layer 213).

The magnetic barrier layer 224 is of a material having relatively high paramagnetic properties such as for example, Cu, or Al, and covers at least the flipping layers 209, 211 to shield them from external magnetic signals that may cause incorrect writes; and also may stop magnetic interference signals emanating from the flipping layers 209, 211. Preferably, the magnetic barrier layer 224 fully encapsulates the MRAM structure 200 from an upper surface 225 of the substrate 201 to a side wall 227 or lower surface 229 of the cap layer 213. The magnetic barrier layer 224 may be of any suitable material having relatively high paramagnetic properties such as, for example, copper or a compound of copper having a high copper content.

The magnetic barrier layer 224 may be applied using known techniques such as, for example, plating or sputtering, after applying a photoresist layer to those surfaces not requiring the magnetic barrier layer 224 (e.g. the top of free layer 211 or cap layer 213).

Therefore, the MRAM structure 200 is shielded from external interference by the eddy current side wall 221, the cap layer 213 and the substrate 201. The

external interference may be from one or more adjacent cells or from another source such as, for example, a power supply.

Figure 3 shows a variation. Here, only the flipping layers 309, 311 having
5 applied thereto the eddy current side wall 321. There is no eddy current side wall 321 over the pinning layers 313, 305 or the insulating layer 307. The structure of the eddy current side wall 321 is the same and it is formed in the same manner as described above. The photoresist would therefore be applied to the side walls of the pinning layers 303, 305 as well as the insulating layer
10 307.

In both exemplary embodiments, the MRAM structure 200, 300 should not suffer from one or more of:

- the half-select or write disturb problem;
- 15 eddy current tunneling during fast write cycles;
- eddy current leakage to an adjacent cell;
- magnetic stray field interference; and
- imperfect anisotropy uniformity during thermal conditions.

20 Furthermore, the addition of the eddy current side wall 221, 321 may:

- reduce potential interference between cells both magnetically and electrically;
- enable higher density MRAM as it will permit closer cell spacing; and
- improve per wafer density.

Whilst the foregoing description has described exemplary embodiments, it will be understood by those skilled in the technology concerned that many variations in details of design, construction and/or operation may be made
5 without departing from the present invention.

The Claims:

1. A magnetoresistive random access memory ("MRAM") device
comprising:
a plurality of layers on a substrate, the plurality of layers comprising
pinning layers, flipping layers, and at least one insulating layer between
the pinning layers and the flipping layers; and
an eddy current side wall encapsulating at least the pinning layers of
the plurality of layers, the eddy current side wall comprising a grain
insulating layer for electrical insulation, and a magnetic barrier layer for
magnetic isolation.
2. A MRAM device as claimed in claim 1 further comprising a cap layer on
the plurality of layers remote from the substrate.
3. A MRAM device as claimed in claim 2, wherein the eddy current side wall
extends between the substrate and the cap layer for reducing potential
interference both magnetically and electrically.
4. A magnetoresistive random access memory ("MRAM") device
comprising:
a plurality of layers on a substrate, the plurality of layers comprising
pinning layers, flipping layers, and at least one insulating layer between
the pinning layers and the flipping layers;
a cap layer over the plurality of layers remote from the substrate; and

an eddy current side wall encapsulating and insulating the plurality of layers, the eddy current side wall extending from and between the cap layer and the substrate.

5 5. A MRAM device as claimed in claim 2 or claim 4, wherein the eddy current side wall extends between an upper surface of the substrate to at least one of a side wall and a lower surface of the cap layer.

10 6. A MRAM device as claimed in any one of claims 1 to 3, wherein the magnetic barrier layer comprises a material having relatively high paramagnetic properties.

15 7. A MRAM device as claimed in claim 6, wherein the material is selected from the group consisting of: copper, and a compound of copper having a high copper content.

20 8. A MRAM device as claimed in any one of claims 1 to 3, 6 or 7, wherein the grain insulating layer comprises at least one selected from the group consisting of: an O_3 compound, and an O_3 compound of a metal.

9. A MRAM device as claimed in claim 8, wherein the grain insulating layer is selected from the group consisting of: Al_2O_3 , Fe_2O_3 and B_2O_3 .

10. A MRAM device as claimed in any one of claims 6 to 9, wherein the grain insulating layer is over the flipping layers, and the magnetic barrier layer is over the grain insulating layer.

5 11. A method of insulating a magnetoresistive random access memory ("MRAM") device, the MRAM device comprising a plurality of layers on a substrate, the plurality of layers comprising pinning layers, flipping layers, and at least one insulating layer between the pinning layers and the flipping layers; the method comprising:

10 forming an eddy current side wall encapsulating at least the pinning layers of the plurality of layers, the eddy current barrier being formed by first forming one of a grain insulating layer for electrical insulation and a magnetic barrier layer for magnetic isolation, then forming the other of the grain insulating layer for electrical insulation and the magnetic barrier
15 layer for magnetic isolation.

12. A method as claimed in claim 11, wherein the grain insulating layer for electrical insulation is formed over side walls of at least the plurality of flipping layers and the magnetic barrier layer is formed over the grain
20 insulating layer.

13. A method as claimed in claimed in claim 11 or claim 12, wherein before forming the eddy current side wall, a photoresist layer is formed over

those surfaces where the eddy current side wall is not required; the eddy current side wall being formed by one of: plating, and sputtering.

14. A method as claimed in any one of claims 11 to 13 further comprising
5 forming a cap layer on the plurality of layers remote from the substrate.

15. A method as claimed in claim 14, wherein the eddy current side wall is formed between the substrate and the cap layer for reducing potential interference both magnetically and electrically.

10 16. A method as claimed in claim 15, wherein the eddy current side wall is formed between an upper surface of the substrate to at least one of a side wall and a lower surface of the cap layer.

15 17. A method as claimed in any one of claims 11 to 16, wherein the magnetic barrier layer comprises a material having relatively high paramagnetic properties.

18. A method as claimed in claim 17, wherein the material is selected from the group consisting of: copper, and a compound of copper having a high
20 copper content.

19. A method as claimed in any one of claims 11 to 18, wherein the grain insulating layer comprises at least one selected from the group consisting of: an O_3 compound, and an O_3 compound of a metal.

20. A method as claimed in claim 19, wherein the grain insulation layer is selected from the group consisting of: Al_2O_3 , Fe_2O_3 and B_2O_3 .