

DESCRIPTION

Title of Invention

LEAD FRAME, LEAD FRAME PACKAGE, AND METHOD FOR
MANUFACTURING SAME

5 Technical Field

[0001] The present disclosure relates to a lead frame, a lead frame package, and a method for manufacturing the same.

Background Art

10 [0002] A lead frame package includes a lead frame, a semiconductor chip mounted on the lead frame, and a sealing resin for sealing the semiconductor chip. In the manufacturing of the lead frame package, the lead frame and the semiconductor chip mounted thereon are covered with a thermosetting resin which is cured by heating. In order to
15 secure reliability of the lead frame package, there is known a technique of roughening the surface of the lead frame to improve adhesiveness between the lead frame and the sealing resin.

20 [0003] As the lead frame packages, there is a type in which lead terminals or pads for mounting a semiconductor chip are exposed from a package surface. In the case of this type, if an exposed portion is roughened, a resin leaks to the exposed surface during the sealing with a resin, and thus, resin burrs are likely to occur. It is usually difficult to remove such resin burrs in the manufacturing process, and there is a problem in that the exposed surface is covered with the resin. In addition, when mounting the lead frame package on the board, the lead
25 frame package and the board are electrically conducted to each other by solder. In this case, the lead frame is in contact with the sealing resin

on one main face and in contact with the solder on the other main face. For this reason, each main face is required to be excellent in adhesiveness to the sealing resin and solder.

[0004] Therefore, Patent Literature 1 has proposed a technique of preventing resin burrs and improving adhesiveness to a resin and solder by depositing a rough plating film on one main face of a workpiece and depositing a smooth plating film on the other main face.

Citation List

Patent Literature

[0005] Patent Literature 1: Japanese Unexamined Patent Publication No. 2014-221941

Summary of Invention

Technical Problem

[0006] The lead frame usually has a concavo-convex structure and a through-hole formed by punching or etching treatment or the like. The lead frame where the concavo-convex structure and the through-hole are formed has a pair of main faces and a side face perpendicular thereto. In some cases, a sealing resin may be provided not only on the main face of the lead frame but also on the side face. For this reason, Patent Literature 1 has proposed to provide a plating film also on the side face. However, with the technique of Patent Literature 1, it is difficult to adjust the roughness of the side face of the lead frame.

[0007] Accordingly, an object of the present invention is to provide a method of manufacturing a lead frame capable of easily adjusting roughness of a side face. Another object of the present invention is to provide a lead frame, a lead frame package and a manufacturing method

thereof, which are excellent in reliability.

Solution to Problem

[0008] The present invention provides a method of manufacturing a lead frame including a lead frame main body and a plating film on a surface thereof, the method including a plating step of performing plating treatment to dispose a first electrode connected to a polarity inversion power source so as to face a first main face of a lead frame main body and to dispose a second electrode connected to a pulse power source so as to face a second main face opposite to the first main face and forming the plating film on the first main face, the second main face, and a side face of the lead frame main body.

[0009] The above-described manufacturing method includes the plating step of forming the plating films on the first main face and the second main face of the lead frame main body by using the first electrode connected to the polarity inversion power source and the second electrode connected to the pulse power source. For this reason, the plating films having different roughnesses can be formed on the first main face and the second main face, respectively. Therefore, when resin sealing is performed, the main face having a larger roughness out of the pair of main faces is allowed to be in contact with the resin, and the main face having a lower roughness is allowed to be exposed, a lead frame having a high reliability can be obtained. This is because, while the main face having a larger roughness is excellent in adhesiveness to the resin, the main face having a smaller roughness is able to easily remove the resin burrs, and the bonding area with solder is sufficiently large, so that the heat dissipation can be improved.

[0010] In addition, since the plating step is performed by using the pulse power source, the plating film is formed on the side face of the lead frame main body, mainly by the first electrode connected to the polarity inversion power source during the OFF time of the pulse power source. For example, by prolonging the OFF time, plating formation by the first electrode connected to the polarity inversion power source is further facilitated. Therefore, the roughnesses of the side face of the first main face of the lead frame can be allowed to be sufficiently close to each other. In this manner, it is possible to easily adjust the roughness of the side face.

[0011] The plating film on the first main face may have a larger roughness than the plating film on the second main face. In the pulse power source, the diffusion time of the component (metal ion) to be the plating film is secured, and the occurrence of burning can be sufficiently suppressed. For this reason, the current density to be applied is allowed to be higher than that in the case of using a DC power source, and thus, the crystal grain size of the plating film deposited in the plating step can be allowed to be sufficiently small. Therefore, it is possible to form a plating film having fine texture and sufficiently excellent smoothness on the second main face. By providing such a plating film, separation of the oxide film formed on the surface of the plating film is suppressed. Therefore, it is possible to further improve the reliability of the lead frame.

[0012] In addition, by using a pulse power source, the formation of the plating film by the polarity inversion power source is facilitated on the side face of the lead frame main body. For this reason, the plating film

having a sufficiently larger roughness than that on the second main face can be formed on the side face of the lead frame main body. Therefore, the adhesiveness of the resin on the side face of the lead frame is improved, and thus, it is possible to manufacture a lead frame with more excellent reliability.

[0013] The duty ratio of the pulse power source in the plating step may be 0.2 to 0.85. As a result, while sufficiently securing the difference between the roughness of the plating film on the first main face and the roughness of the plating film on the second main face, the roughness of the plating film on the first main face and the roughness of the plating film on the side face can be brought to be sufficiently close to each other.

[0014] The average current density of the pulse power source in the plating step may be 1 to 10 A/dm². Therefore, it is possible to form the plating film in a short time while sufficiently suppressing occurrence of the plating burning.

[0015] In the plating step, when the roughnesses of the plating film on the first main face, the second main face, and the side face are S_1 , S_2 and S_3 respectively, it is preferable that S_1 is 1.4 or more, S_2 is 1.0 to 1.2, and S_3 is 1.3 or more. Therefore, it is possible to easily remove the resin burrs on the second main face while further improving the adhesiveness between the plating film on the first main face and the side face and the sealing resin in a case where the side face is covered with the sealing resin. In addition, penetration of components such as water vapor from the interface between the side face and the sealing resin can be sufficiently suppressed. Therefore, it is possible to obtain a lead

frame with higher reliability.

[0016] The present invention also provides a method of manufacturing a lead frame package using the lead frame manufactured by the above-described manufacturing method, the method including: a step of providing a semiconductor chip on a first main face of the lead frame; and a step of sealing at least the semiconductor chip with a resin so as to cover the semiconductor chip and the first main face and a side face of the lead frame and to expose at least a portion of a second main face having a smaller roughness than the first main face and the side face of the lead frame.

[0017] In the method of manufacturing the lead frame package, the lead frame manufactured by the method of manufacturing the lead frame described above is used. Then, the method includes a step of sealing so as to cover the semiconductor chip and the first main face and the side face of the lead frame and to expose at least a portion of the second main face having a smaller roughness than the first main face of the lead frame. In this step, at least the semiconductor chip is sealed with the resin so as to expose at least a portion of the second main face having a smaller roughness than the first main face and the side face covered with the resin. Since the second main face has a smaller roughness than the first main face and the side face, the resin burrs are sufficiently removed, so that it is possible to sufficiently increase the bonding area with the solder. Since the first main face and the side face have a larger roughness than the second main face, the first main face and the side face are excellent in adhesiveness to the resin. Therefore, the lead frame package obtained by this manufacturing method has a high

reliability.

[0018] The present invention provides a lead frame including: a lead frame main body; and a plating film on the surface thereof, when roughnesses of plating films on a first main face, a second main face opposite to the first main face, and a side face are denoted by S_1 , S_2 , and S_3 , respectively, S_1 is 1.4 or more, S_2 is in a range of 1.0 and 1.2, and S_3 is 1.3 or more.

[0019] In this lead frame, since the roughness S_2 of the second main face is sufficiently smaller than the roughness S_1 of the first main face, it is possible to easily remove the resin burrs. In addition, since not only the first main face but also the side face has the larger roughness S_3 , the first main face and the side face is excellent in adhesiveness to the sealing resin. For this reason, it is possible to sufficiently expose the second main face while covering the first main face and the side face with the sealing resin. Therefore, it is possible to form a lead frame package excellent in reliability.

[0020] The present invention provides lead frame package including: the above-described lead frame; a semiconductor chip on the first main face thereof; and a sealing resin provided so as to cover the semiconductor chip and the first main face and the side face of the lead frame and to expose at least a portion of the second main face having a smaller roughness than the first main face and the side face of the lead frame. Such a lead frame package has high reliability because the second main face is excellent in heat radiation and the first main face and side face are excellent in adhesiveness to the sealing resin.

Advantageous Effects of Invention

[0021] The present invention can provide a method of manufacturing a lead frame capable of easily adjusting a roughness of a side face. In addition, the present invention can provide a lead frame, a lead frame package and a manufacturing method thereof which are excellent in reliability.

Brief Description of Drawings

[0022] Fig. 1 is a cross-sectional diagram of a lead frame package.

Fig. 2 is a bottom diagram of the lead frame package.

Fig. 3 is an enlarged cross-sectional diagram illustrating a portion of a cross section of a lead frame.

Fig. 4 is a diagram describing a plating step.

Fig. 5 is a diagram describing a plating step.

Fig. 6 is a diagram illustrating a profile of a current by a polarity inversion power source during a plating step.

Fig. 7 is a diagram illustrating a profile of a current by a pulse power source during a plating step.

Description of Embodiments

[0023] Hereinafter, some embodiments of the present invention will be described with reference to the drawings as needed. However, the following embodiments are merely examples illustrating the present invention, and it is not intended to limit the present invention to the following contents. In the description, the same reference numerals denote the same components or the components having the same functions, and in some cases, redundant description will be omitted. In addition, positional relationships such as up, down, left, and right are based on positional relationships illustrated in the drawings unless

otherwise specified. In addition, dimensional ratios of members are not limited to illustrated ratios.

[0024] Fig. 1 is a cross-sectional diagram of a lead frame package according to this embodiment. A lead frame package 100 includes a so-called QFN type lead frame 10. That is, the lead frame package 100 includes a lead frame 10 having an electrode pad 10A and leads 10B arranged around the electrode pad 10A, a semiconductor chip 20 provided on one main face 10a (first main face 10a) of the electrode pad 10A, a bonding wire 22 connecting the semiconductor chip 20 and the lead 10B, and a sealing resin 60 sealing the semiconductor chip 20 and the bonding wire 22. The sealing resin 60 is provided so as to cover the semiconductor chip 20 and one main face 10a and a portion of a side face 10c of the lead frame 10.

[0025] Fig. 2 is a bottom diagram of the lead frame package 100 of Fig. 1. One main face 10a and side face 10c of the lead frame 10 are covered with the sealing resin 60, whereas the other main face 10b (second main face 10b) of the lead frame 10 is not covered with the sealing resin 60 but exposed to the outside. The surface of the lead frame 10 is configured with a plating film. The main face 10b has a smaller roughness than the main face 10a and the side face 10c and has smoothness.

[0026] In a case where the lead frame package 100 is mounted on a board such as a printed wiring board or the like, the main face 10b of the lead frame 10 is connected to a conductor of the printed wiring board by solder. Since the roughness of the main face 10b of the lead frame 10 is sufficiently small, even if a resin composition for forming

the sealing resin 60 adheres to the main face 10b of the lead frame 10, the sealing resin can be removed easily. Therefore, in a case where the lead frame package is mounted on the board, a bonding area between the main face 10b and the solder is sufficiently increased, so that it is possible to exhibit excellent heat dissipation.

[0027] A roughness S_2 of the main face 10b of the lead frame 10 is preferably 1.0 to 1.2, more preferably 1.0 to 1.15. That is, the main face 10b is configured with a plating film having such a roughness. In this specification, the "roughness" is an S-ratio measured with a shape measuring laser microscope (manufactured by Keyence Corporation, trade name: VK-X 200, observation area: about $100\ \mu\text{m}^2$). The S-ratio is an area ratio calculated by dividing an area including irregularities by an observation area.

[0028] In the process of manufacturing the lead frame package 100 by using the lead frame 10, when the semiconductor chip 20 is to be mounted on the electrode pad 10A, when the semiconductor chip 20 and the lead 10B are to be connected to each other by a bonding wire 22, and when the sealing resin 60 is to be formed by heating and curing a thermosetting resin, the lead frame 10 is exposed to heat. By such heat, an oxide film is formed on the surface of the plating film. Since the main face 10b of the lead frame 10 is configured with a plating film of which roughness is sufficiently small, peeling of the oxide film can be suppressed.

[0029] In addition, in a case where the plating film on the main face 10b is formed by an electrode connected to a pulse power source, it is possible to allow a crystal grain size constituting the plating film to be

sufficiently small. Therefore, voids generated during the formation of the oxide film are reduced, and as a result, it is possible to further suppress peeling of the oxide film.

[0030] At least a portion of the one main face 10a and the side face 10c of the lead frame 10 is in contact with the sealing resin 60. The one main face 10a and the side face 10c of the lead frame 10, which is in contact with the sealing resin 60, has a larger roughness than the main face 10b. Therefore, the one main face 10a and the side face 10c of the lead frame 10 are excellent in adhesiveness to the sealing resin 60.

[0031] The roughness S_1 of the main face 10a of the lead frame 10 is preferably 1.4 or more, more preferably 1.5 or more. Therefore, it is possible to allow the adhesiveness between the main face 10a and the sealing resin 60 to be sufficiently high. On the other hand, the upper limit of the roughness S_1 of the main face 10a is also not particularly limited and, for example, may be 4 or less or may be 3.5 or less. Therefore, it is possible to sufficiently increase the adhesiveness between the main face 10a and the semiconductor chip 20 and the adhesiveness between the main face 10a and the bonding wire 22. The main face 10a is configured with a plating film having such a roughness S_1 . The roughness S_1 is measured in the same manner as the roughness S_2 .

[0032] The roughness S_3 of the side face 10c of the lead frame 10 is preferably 1.3 or more, more preferably 1.5 or more. Therefore, it is possible to sufficiently increase the adhesiveness between the side face 10c and the sealing resin 60 and to sufficiently suppress penetration of such a component as water vapor from the interface between the side

face 10c and the sealing resin 60. The upper limit of the roughness S_3 of the side face 10c of the lead frame 10 is also not particularly limited, and for example, may be the roughness S_1 of the main face 10a or less or 4 or less, or may be 3.5 or less. The side face 10c is configured with a plating film having the above-mentioned roughness S_3 . The roughness S_3 is measured in the same manner as the roughness S_1 and S_2 .

[0033] When the lead frame 10 is used, the main face 10a and the side face 10c are allowed to be in close contact with the sealing resin 60, and the main face 10b having a roughness sufficiently smaller than the main face 10a is exposed, so that it is possible to manufacture the lead frame package 100. The main face 10a and the side face 10c are excellent in adhesiveness to the sealing resin 60, and the main face 10b is excellent in solderability and heat dissipation. Therefore, it is possible to manufacture the lead frame package 100 having excellent reliability.

[0034] The lead frame package 100 has high reliability because the main face 10b of the lead frame 10 is excellent in solderability and heat dissipation and the main face 10a and the side face 10c are excellent in adhesiveness to the sealing resin 60.

[0035] In some embodiments, from the viewpoint of further increasing the reliability, it is preferable to satisfy the following formula (1). In addition, it is preferable that S_1 , S_2 , S_3 satisfy the relationship of the following formula (2). In addition, from the viewpoint of allowing the roughness S_1 of the main face 10a to be sufficiently larger than the roughness S_2 of the main face 10b, the following formula (3) may be satisfied.

$$0.58 < S_3/S_1 \leq 1 \quad (1)$$

$$S_2 < S_3 \leq S_1 \quad (2)$$

$$S_2/S_1 < 0.6 \quad (3)$$

[0036] Since the roughness S_3 of the side face 10c is approximately equal to the roughness S_1 of the main face 10a, the lead frame 10 is excellent in adhesiveness to the sealing resin 60 on the main face 10a and the side face 10c. By allowing the roughness S_2 of the main face 10b to be sufficiently smaller than the roughness S_1 of the main face 10a, the exposed area is sufficiently increased by removing the resin burrs, so that it is possible to improve the heat dissipation.

[0037] From the viewpoint of further increasing the reliability, in the above formula (1), S_3/S_1 may be 0.6 or more or may be 0.7 or more. In the above formula (3), S_2/S_1 may be less than 0.5. The lower limit of S_2/S_1 is not particularly limited, but the lower limit may be 0.3 or may be 0.4.

[0038] Fig. 3 is an enlarged cross-sectional diagram illustrating a portion of the cross section of the lead frame 10 (the electrode pad 10A or the lead 10B). The lead frame 10 includes a lead frame main body 11 and a plating film 12 covering the surface of the lead frame main body 11. The lead frame main body 11 is made of, for example, copper or a copper alloy. The thickness of the plating film 12 is, for example, 0.2 to 3 μm . The plating film 12 is configured with one or a plurality of metal layers made of, for example, at least one metal selected from a group including nickel, copper, palladium, silver, and gold or an alloy of the metal. More specifically, an electrolytic plating film having only a copper plating layer and an electrolytic plating film

obtained by laminating a nickel layer/a palladium layer/a gold layer may be exemplified. In the case of a copper plating layer, a silver plating layer may be formed partially on the copper plating layer, that is, on a connection portion with the bonding wire 22 or the like.

5 [0039] A plating film 12 is formed on the main faces 11a and 11b and the side face 11c of the lead frame main body 11. Plating films 12 having different roughnesses are formed on the main face 11a, the main face 11b, and the side face 11c, respectively. The plating films 12 having different roughnesses can be formed on the main face 11a, the
10 main face 11b, and the side face 11c by a plating step described later.

[0040] Next, a method of manufacturing the lead frame 10 and the lead frame package 100 will be described. This manufacturing method includes a plating step of forming the plating film 12 on the lead frame main body 11. More specifically, first, a metal sheet made of copper or
15 the like is punched out to form a lead frame main body 11 having a predetermined shape. Subsequently, the surface of the lead frame main body 11 is covered with a plating film using a plating solution.

[0041] Figs. 4 and 5 are diagrams describing the plating step. As illustrated in Fig. 4, the lead frame main body 11 continuously passes
20 through the plating tank 50. Fig. 5 illustrates a cross section when the plating tank 50 and the lead frame main body 11 (lead frame 10) passing through the inside of the plating tank 50 are cut along a plane perpendicular to the passing direction of the lead frame main body 11 (lead frame 10).

25 [0042] As illustrated in Fig. 5, a plating solution 52 is stored in the plating tank 50. The lead frame main body 11 is immersed in the

plating solution 52 and subjected to electrolytic plating treatment to form an electrolytic plating film on the surface of the lead frame main body 11. Therefore, the lead frame 10 is obtained. As the plating solution 52, a copper plating solution, a nickel plating solution, a palladium plating solution, a gold plating solution, or the like may be used. In the case of forming a plating film configured with a plurality of layers, a plurality of the plating tanks 50 may be arranged in series along the passing direction of the lead frame main body 11, and plating treatment may be continuously performed.

[0043] As illustrated in Fig. 5, in the plating tank 50, a pair of electrodes 32 and 42 having a flat plate shape are arranged so as to interpose the lead frame main body 11. The one electrode 32 (first electrode 32) is arranged to face the main face 11a of the lead frame main body 11, and the other electrode 42 (second electrode 42) is arranged to face the main face 11b of the lead frame main body 11. The electrode 32 is connected to the polarity inversion power source 30, and the electrode 42 is connected to the pulse power source 40.

[0044] Fig. 6 is a diagram illustrating a profile of a current by the polarity inversion power source 30 during the plating step. In the plating step, the positive current A1 and the negative current A2 are alternately supplied from the polarity inversion power source 30 to the electrode 32. When the positive current is supplied from the polarity inversion power source 30, the plating film 12 is formed on the main face 11a of the lead frame main body 11. On the other hand, when the negative current is supplied from the polarity inversion power source 30, a portion of the plating film 12 on the main face 11a is eluted into the

plating solution 52 by anodic electrolysis. The roughness of the plating film 12 can be controlled by adjusting the magnitudes of the positive current A1 and the negative current A2, the positive current time t1, and the negative current time t2.

5 [0045] For example, the plating film 12 having a large roughness can be formed by forming a plating film with a positive current larger than a positive current capable of forming a smooth plating film and by dissolving the grain boundary portion of the plating film at the time of supplying the negative current.

10 [0046] The positive current density may be set within a range of, for example, 5 to 20 A/dm². The negative current density may be set to be larger than the positive current density and may be set within a range of, for example, 20 to 50 A/dm². The positive current time t1 and the negative current time t2 may be set within a range of, for example, 1 to
15 100 milliseconds.

[0047] Fig. 7 is a diagram illustrating a profile of the current by the pulse power source 40 during the plating step. In the plating step, a positive pulse current is supplied from the pulse power source 40 to the electrode 42. When a positive pulse current is supplied from the
20 polarity inversion power source 30, the plating film 12 is formed on the main face 11b of the lead frame main body 11. Since the plating film is not formed while the supply of the positive pulse current is stopped, it is possible to secure the time for metal ions, which are to constitute the plating film, to be diffused in the vicinity of the main face 11b of the
25 lead frame main body 11. Therefore, the burning of the plating film 12 hardly occurs. Therefore, the peak current value B1 of the positive

pulse current of the pulse power source 40 is allowed to be sufficiently large, so that it is possible to form the plating film 12.

[0048] The plating film 12 is formed by sufficiently increasing the current density of the positive pulse current by the pulse power source 40, so that it is possible to sufficiently reduce the crystal grain size of the metal particles constituting the plating film 12. Therefore, it is possible to form the plating film 12 having excellent smoothness on the main face 11b of the lead frame main body 11. Since such a plating film 12 is configured with sufficiently small crystal grains, it is possible to sufficiently suppress the peeling of the oxide film formed on the surface of the plating film 12.

[0049] In the manufacturing process of the lead frame 10 and the lead frame package 100, according to the heating, the metal components of the lead frame main body 11 and the plating film 12 are diffused into the surface to form an oxide film. In the present embodiment, since the crystal grain size of the plating film 12 is small, it is possible to reduce the amount and size of voids between the lead frame main body 11 and the plating film 12 caused by the diffusion. Therefore, it is possible to sufficiently suppress the peeling of the oxide film formed on the surface of the plating film 12 on the main face 11b.

[0050] In the plating step, it is possible to simultaneously form the plating film 12 on the main face 11a and the main face 11b of the lead frame main body 11 by concurrently supplying the current from the polarity inversion power source 30 and the pulse power source 40. In addition, it is possible to form the plating film 12 on the side face 11c of the lead frame main body 11 at the same time.

[0051] The roughness S_3 of the plating film 12 on the side face 11c can be adjusted by adjusting the duty ratio and the current density of the pulse power source 40. In the case of the current profile illustrated in Fig. 7, the duty ratio of the pulse power source 40 is calculated as $t_4/(t_3 + t_4)$. t_4 is a time (ON time) during which the pulse current is supplied, and t_3 is a time (OFF time) during which the supplying of the pulse current is stopped.

[0052] While no current is supplied from the pulse power source 40 to the electrode 42, the plating film 12 is formed on the side face 11c by the positive current A1 supplied from the polarity inversion power source 30 to the electrode 32. The rate of formation of the plating film 12 by the positive current from the polarity inversion power source 30 is higher than that in the case of using a DC power source instead of the pulse power source 40. Therefore, it is possible to allow the roughness S_3 of the plating film 12 on the side face 11c to be large.

[0053] From the viewpoint of sufficiently increasing the roughness of the plating film 12 on the side face 11c, the duty ratio of the pulse power source 40 is preferably 0.85 or less, more preferably 0.7 or less. On the other hand, if the duty ratio of the pulse power source 40 is too small, the ratio of the plating film 12 formed by the positive current A1 from the polarity inversion power source 30 to the main face 11b as well as the side face 11c is increased. Therefore, from the viewpoint of maintaining the roughness S_2 on the main face 11b sufficiently small, the duty ratio of the pulse power source 40 is preferably 0.2 or more, more preferably 0.3 or more.

[0054] The average current density of the pulse power source 40 may

be 1 to 10 A/dm² or may be 1 to 5 A/dm². Therefore, it is possible to sufficiently suppress the occurrence of the plating burning on the main face 10b, and it is possible to allow the crystal grain diameter constituting the plating film 12 on the main face 10b to be sufficiently small. In addition, it is possible to form the plating film 12 in a short time. The average current density of the pulse power source 40 can be obtained by converting the average current value B2 (Fig. 7) of the current supplied from the pulse power source 40 into the current density. The average current value B2 is obtained as a product of the peak current value B1 of the positive pulse current and the duty ratio.

[0055] By the plating step as described above, it is possible to form the plating film 12 having a larger roughness than the main face 11b on the main face 11a and the side face 11c of the lead frame main body 11. In this plating step, it is possible to easily adjust the roughness of the side face 10c of the lead frame 10 by changing the duty ratio or the average current density. The roughnesses S₁, S₂, and S₃ of the plating film 12 on the main face 11a, the main face 11b, and the side face 11c may satisfy, for example, the above-described formulas (1), (2), and (3).

[0056] The semiconductor chip 20 is fixed to the main face 10a side of the electrode pad 10A of the lead frame 10 obtained in the plating step by using a metal paste such as a silver paste. Next, the electrode pad (not shown) of the semiconductor chip 20 and the main face 10a of the lead 10B are connected to each other by the bonding wire 22. Subsequently, the lead frame 10 is disposed within a mold. Then, a resin composition (for example, a thermosetting resin composition such as an epoxy resin) is injected into the mold and heated to cure the resin

composition. Thereafter, by dicing, the lead frame package 100 including the semiconductor chip 20 mounted on the lead frame 10 and the sealing resin 60 sealing the bonding wire 22 connecting the semiconductor chip 20 and the lead 10B is obtained.

5 [0057] The above-described lead frame package 100 includes the lead frame 10 having the main face 10a and the side face 10c having large roughness. The lead frame 10 is excellent in adhesiveness to the sealing resin 60 and also excellent in heat dissipation. In addition, the lead frame 10 can sufficiently suppress peeling of the oxide film formed
10 on the main face 10b. Therefore, the lead frame package 100 has high reliability.

[0058] Heretofore, although the embodiment of the present invention has been described above, the present invention is not limited to the above embodiment. For example, in the above embodiment, although
15 the lead frame is of the QFN type, the invention is not limited thereto, but the lead frame may be of a DFN type, and the lead frame package may be a pad exposure type QFP package or the like. In addition, in the above embodiment, although the plating film 12 having a larger roughness than the main face 11b of the lead frame main body is formed
20 on the main face 11a and the side face 11c of the lead frame main body facing the electrode 32 connected to the polarity inversion power source 30, the present invention is not limited thereto. A plating film 12 having a larger roughness than the plating film 12 on the main face 11a and the side face 11c of the lead frame main body may be formed on the
25 main face 11b of the lead frame main body 11 facing the electrode 42 connected to the pulse power source 40. In this case, the plating film

12 on the main face 11b of the lead frame main body 11 is excellent in adhesiveness to the resin, and the plating film 12 on the main face 11a and the side face 11c of the lead frame main body 11 is excellent in adhesiveness to the solder.

5 [0059] Such a lead frame can be manufactured, for example, as follows. The plating film 12 is formed on the main face 11a of the lead frame main body 11 with a positive current of a size large enough to form a smooth plating film by using the polarity inversion power source 30, and convex portions of the plating film 12 are intensively electrolyzed
10 with a negative current. Therefore, the plating film 12 having a smaller roughness than the plating film 12 on the main face 11b can be formed on the main face 11a and the side face 11c.

Example

15 [0060] The contents of the present invention will be described in more detail with reference to Examples and Comparative Examples, but the present invention is not limited to the following Examples.

[0061] (Example 1)

[Formation of Plating Film]

20 A lead frame main body made of a copper alloy was prepared. Electroplating treatment was performed by using a plating apparatus as illustrated in Figs. 4 and 5 to form a copper plating film (thickness: 0.6 to 0.8 μm) on the surface of the lead frame main body to manufacture a lead frame. The thickness of the copper plating film was measured by using a fluorescent X-ray film thickness meter (manufactured by
25 Helmut Fischer GmbH, product name: FISCHER SCOPE X-RAY XDV- μ). As the plating solution, a plating solution containing copper

sulfate (160 g/L) and sulfuric acid (75 g/L) as main components was used. As the polarity inversion power source and the pulse power source, commercially available ones were used. The operating conditions of the power sources were as follows.

5 [0062] <Polarity inversion power source>

Positive current density: 10.9 A/dm^2

Negative current density: 31.6 A/dm^2

Positive current time (t1): Negative current time (t2) = 25 ms : 4
ms

10 <Pulse power source>

Peak current density: 10 A/dm^2

Average current density: 2.5 A/dm^2

ON time (t3): OFF time (t4) = 25 msec : 75 msec

(Duty ratio = 0.25)

15 [0063] [Evaluation of Copper Plating Film]

By using a commercially available shape measuring laser microscope (manufactured by Keyence Corporation, product name: VK-X 200), the roughness S_1 of the first main face (the main face facing the electrode connected to the polarity inversion power source) of the
20 lead frame, the roughness S_2 of the second main face (the main face facing the electrode connected to the pulse power source), and the roughness S_3 of the side face were measured. The measurement results are illustrated in Table 1.

[0064] (Comparative Example 1)

25 A lead frame was manufactured in the same manner as in Example 1 except that a DC power source was used instead of the pulse

power source. In addition, the current density of the DC power source was adjusted to 5.0 A/dm² so that the roughness S₂ of the second main face was the same as that of Example 1. The roughness S₁ of the first main face (the main face facing the electrode connected to the polarity inversion power source) of the obtained lead frame, the roughness S₂ of the second main face (the main face facing the electrode connected to the DC power source), and the roughness S₃ of the side face were measured in the same manner as in Example 1. The measurement results are illustrated in Table 1.

[0065] [Table 1]

	Roughness S ₁ of the first main face	Roughness S ₂ of the second main face	Roughness S ₃ of the side face	S ₃ /S ₁	S ₃ /S ₂	S ₂ /S ₁
Example 1	2.232	1.108	1.782	0.798	1.608	0.496
Comparative Example 1	2.305	1.106	1.286	0.558	1.163	0.480

[0066] From the results in Table 1, it was understood that, by using the pulse power source, the roughness S₃ of the side face can be allowed to be sufficiently large so as to be close to the roughness S₁ of the first main face. The lead frame of Example 1 was excellent in adhesiveness to the resin on the first main face and the side face, and thus, the resin burrs on the second main face was able to be easily removed.

[0067] (Example 2)

A plating film was formed in the same manner as in Example 1 except that the operating conditions of the pulse power source were changed as follows. The thickness of the copper plating film formed on the surface of the lead frame main body was 0.7 μm. The copper

plating film was evaluated in the same manner as in Example 1. The results are illustrated in Table 2.

<Pulse power source>

Average current density: 2.5 A/dm³

5 ON time (t3) : OFF time (t4) = 50 msec : 50 msec

(Duty ratio = 0.5)

[0068] After the above evaluation, a heating test was performed in the air, and a peeling test of the oxide film was performed. More specifically, after heating under the heating conditions listed in Table 2, cooling was performed, and a commercially available tape (manufactured by Sumitomo 3M Ltd., trade name: Scotch (registered trademark) Mending Tape 810) was attached to the second main face of the lead frame. Thereafter, the attached tape was peeled off, and the presence or absence of peeling of the oxide film was visually evaluated. The plating film where no peeling occurred was evaluated as "A" and the plating film where peeling occurred was evaluated as "B". The evaluation results are illustrated in Table 2.

[0069] (Comparative Example 2)

20 A copper plating film was formed in the same manner as in Comparative Example 1 except that the current density of the DC power source was adjusted to 2.5 A/dm² so that the thickness of the copper plating film on the second main face was the same as (0.7 μm) as that of Example 2. Then, evaluation was performed in the same manner as in Example 2. The evaluation results are illustrated in Table 2.

25 [0070] [Table 2]

	300°C	320°C	360°C	380°C	360°C	340°C
	For 5 min	For 5 min	For 5 min	For 5 min	For 10 min	For 20 min
Example 2	A	A	A	A	A	A
Comparative Example 2	A	A	A	B	B	B

[0071] The peeling suppression performance of the oxide film is improved as the thickness of the plating film is increased. From the results in Table 2, it was understood that, in comparison of Example 2 and Comparative Example 2 having the same thickness of the plating film, Example 2 can suppress peeling of the oxide film more than Comparative Example 2. This is because the structure of the plating film on the second main face is becomes fine in Example 2.

[0072] (Examples 3 and 4)

A plating film was formed and evaluated in the same manner as in Example 1 except that the operating conditions of the pulse power source were changed as follows. More specifically, by setting the peak current density to 10 A/dm², setting the ON time (t₃) to 25 milliseconds, and changing the OFF time (t₄), the effect of the duty ratio was examined. A lead frame manufactured under the condition that the duty ratio of the pulse power source was 0.20 (average current density: 2 A/dm²) was taken as Example 3. A lead frame manufactured under the condition that the duty ratio of the pulse power source was 0.83 (average current density: 8.3 A/dm²) was taken as Example 4. The obtained lead frames of respective Examples were evaluated in the same manner as in Example 1. The results are illustrated in Table 3.

[0073] [Table 3]

	Roughness S_1 of the first main face	Roughness S_2 of the second main face	Roughness S_3 of the side face	S_3/S_1	S_3/S_2	S_2/S_1
Example 3	2.287	1.144	1.695	0.741	1.482	0.500
Example 4	2.519	1.120	1.507	0.598	1.346	0.445

[0074] From the results illustrated in Table 3, it was understood that, even if the duty ratio is changed, it is possible to obtain a lead frame in which the roughnesses S_1 and S_3 of the first main face and the side face are sufficiently large and the roughness S_2 of the second main face is sufficiently small. The first main faces and side faces of the lead frames of Examples 3 and 4 were excellent in adhesiveness to the resin, and the second main face was able to easily remove the resin burrs.

[0075] (Example 5)

A plating film was formed and evaluated in the same manner as in Example 1 except that the operating conditions of the pulse power source were changed as follows. More specifically, by setting the ON time (t_3) to 25 milliseconds, setting the OFF time (t_4) to 5 milliseconds, and changing to the peak current value B1 of the positive pulse current, the lead frame was manufactured under the condition that the average current density is 1.0 A/cm². The obtained lead frame of Example 5 was evaluated in the same manner as in Example 1. The results are illustrated in Table 4.

[0076] [Table 4]

	Roughness S_1 of the first main face	Roughness S_2 of the second main face	Roughness S_3 of the side face	S_3/S_1	S_3/S_2	S_2/S_1
Example 5	2.521	1.152	1.549	0.614	1.345	0.457

[0077] From the results in Table 4, it was understood that, even if the

average current density is changed, it is possible to obtain a lead frame in which the roughnesses S_1 and S_3 of the first main face and side faces are sufficiently large and the roughness S_2 of the second main face is sufficiently small. It was understood that, if the average current density was reduced, the roughness S_3 on the side face tended to increase. The first main face and the side face of the lead frame of Example 5 were excellent in adhesiveness to the resin, and thus, the second main face was able to easily remove the resin burrs.

Industrial Applicability

[0078] A method of manufacturing a lead frame capable of easily adjusting roughness of a side face is provided. A lead frame, a lead frame package and a manufacturing method thereof excellent in reliability are provided.

Reference Signs List

[0079] 10: lead frame, 10A : electrode pad, 10B : lead, 10a : main face (first main face), 10b : main face (second main face), 10c : side face, 11 : lead frame main body, 11a : main face (first main face), 11b : main face (second main face), 11c : side face, 12 : plating film, 20 : semiconductor chip, 22 : bonding wire, 30 : polarity inversion power source, 32 : electrode (first electrode), 40 : pulse power source, 42 : electrode (second electrode), 50 : plating tank, 52 : plating solution, 60 : sealing resin, 100 : lead frame package.

CLAIMS

1. A method of manufacturing a lead frame including a lead frame main body and a plating film on a surface thereof, the method comprising:

5 a plating step of

performing plating treatment to dispose a first electrode connected to a polarity inversion power source so as to face a first main face of a lead frame main body and to dispose a second electrode connected to a pulse power source so as to face a second main face opposite to the first main face and

10

forming the plating film on the first main face, the second main face, and a side face of the lead frame main body.

2. The method of manufacturing a lead frame according to claim 1, wherein the plating film on the first main face has a larger roughness than the plating film on the second main face.

15

3. The method of manufacturing a lead frame according to claim 1 or 2, wherein the duty ratio of the pulse power source in the plating step is 0.2 to 0.85.

4. The method of manufacturing a lead frame according to any one of claims 1 to 3, wherein the average current density of the pulse power source in the plating step is 1 to 10 A/dm².

20

5. The method of manufacturing a lead frame according to any one of claims 1 to 4, wherein, when roughnesses of the plating films on the first main face, the second main face and the side face are denoted by S₁, S₂, and S₃, respectively, S₁ is 1.4 or more, S₂ is in a range of 1.0 and 1.2, and S₃ is 1.3 or more.

25

6. The method of manufacturing a lead frame according to claim 5,

wherein $S_3/S_1 < 1$ is satisfied.

7. A method of manufacturing a lead frame package using the lead frame manufactured by the manufacturing method according to any one of claims 1 to 6, the method of manufacturing a lead frame package comprising:

a step of providing a semiconductor chip on a first main face of the lead frame; and

a step of sealing at least the semiconductor chip with a resin so as to cover the semiconductor chip and the first main face and a side face of the lead frame and to expose at least a portion of a second main face having a smaller roughness than the first main face and the side face of the lead frame.

8. A lead frame comprising:

a lead frame main body; and

a plating film on a surface thereof,

wherein, when roughnesses of plating films on a first main face, a second main face opposite to the first main face, and a side face are denoted by S_1 , S_2 , and S_3 , respectively, S_1 is 1.4 or more, S_2 is in a range of 1.0 and 1.2, S_3 is 1.3 or more, and $S_3/S_1 < 1$ is satisfied.

9. A lead frame package comprising:

the lead frame according to claim 8;

a semiconductor chip on the first main face of the lead frame;

and

a sealing resin provided so as to cover the semiconductor chip and the first main face and the side face of the lead frame and to expose at least a portion of the second main face having a smaller roughness than the first main face and the side face of the lead frame.