WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

gate layers and insulating layers that are stacked alternatingly along a first direction perpendicular to a substrate of the semiconductor device and form a stack upon the substrate;

an array of channel structures being formed in an array region of the stack;

a first staircase formed at a first section of the stack in a connection region on the substrate; and

a second staircase formed at a second section of the stack in the connection region on the substrate, wherein:

the first staircase is positioned over the second staircase,

the first staircase includes first group stair steps descending in a second direction parallel to the substrate and first division stair steps descending in a third direction and a fourth direction that are parallel to the substrate and perpendicular to the second direction, the third direction and the fourth direction being opposite to each other, and

the second staircase includes second group stair steps descending in the second direction and second division stair steps descending in the third direction and the fourth direction.

2. The semiconductor device of claim 1, wherein:

a height difference of two consecutive first group stair steps of the first group stair steps in the first direction is equal to a height of N pairs of the gate layers and the insulating layers in the first section, and

a height difference of two consecutive first division stair steps of the first division stair steps in the first direction is equal to a height of one pair of the gate layer and the insulating layer in the first section, the N being greater than one.

3. The semiconductor device of claim 2, further comprising:

a dummy staircase formed at the first section of the stack and disposed between the first staircase and the second staircase in the connection region, wherein:

the dummy staircase ascends in the second direction and has a same height

as the first staircase,

the dummy staircase is positioned over the second staircase, and

the dummy staircase includes dummy group stair steps descending in the second direction, and dummy division stair steps descending in the third direction and the fourth direction.

4. The semiconductor device of claim 1, wherein the first section of the stack and the second section of the stack have a same number of gate layers.

5. The semiconductor device of claim 1, wherein:

a height difference of two consecutive second group stair steps of the second group stair steps in the first direction is equal to a height of N pairs of the gate layers and the insulating layers in the second section, and

a height difference of two consecutive second division stair steps of the second division stair steps in the first direction is equal to a height of one pair of the gate layer and the insulating layer in the second section.

6. The semiconductor device of claim 3, wherein a height difference of two consecutive dummy group stair steps of the dummy group stair steps in the first direction is equal to the height of the N pairs of the gate layers and the insulating layers in the first section.

7. The semiconductor device of claim 5, wherein corresponding group stair steps of the first group stair steps in the first staircase and the second group stair steps in the second staircase are of a same height.

8. The semiconductor device of claim 1, further comprising:

a third staircase formed of a third section of the stack that corresponds to gate top select transistors in the channel structures.

9. The semiconductor device of claim 5, wherein each first group stair step of the first group stair steps is formed of N first division stair steps and each second

group stair step of the second group stair steps is formed of N second division stair steps.

10. The semiconductor device of claim 5, wherein:

each of the first group stair steps corresponds to N respective first division stair steps, and

each of the second group stair steps corresponds to N respective second division stair steps.

11. A method for fabricating a semiconductor device, comprising:

stacking sacrificial layers and insulating layers alternatingly along a first direction perpendicular to a substrate to form a stack upon the substrate;

shaping the sacrificial layers and the insulating layers in a first section of the stack to form a first staircase and a second staircase in the first section of the stack; and

removing a number of the sacrificial layers and the insulating layers of the second staircase to shift each stair step of the second staircase toward the substrate along the first direction into a second section of the stack by a height equal to a height of the number of the sacrificial layers and the insulating layers, wherein:

the first staircase is positioned over the second staircase,

the first staircase includes first group stair steps descending in a second direction parallel to the substrate and first division stair steps descending in a third direction and a fourth direction that are parallel to the substrate and perpendicular to the second direction, the third direction and the fourth direction being opposite to each other,

the second staircase including second group stair steps descending in the second direction and second division stair steps descending in the third direction and the fourth direction.

12. The method of claim 11, wherein:

a height difference of two consecutive first group stair steps of the first group stair steps in the first direction is equal to a height of N pairs of the gate layers and the insulating layers in the first section, and

a height difference of two consecutive first division stair steps of the first division stair steps in the first direction is equal to a height of one pair of the gate layer and the insulating layer in the first section, the N being greater than one.

13. The method of claim 12, wherein the shaping the sacrificial layers and the insulating layers in the first section of the stack further comprises:

forming a dummy staircase between the first staircase and the second staircase at the first section of the stack, wherein:

the dummy staircase ascends in the second direction and has a same height as the first staircase,

the dummy staircase includes dummy group stair steps descending in the second direction, and dummy division stair steps descending in the third direction and the fourth direction, and

a height difference of two consecutive dummy group stair steps of the dummy group stair steps in the first direction is equal to the height of the N pairs of the gate layers and the insulating layers in the first section.

14. The method of claim 11, further comprising:

forming channel structures in the stack in an array region;

replacing the sacrificial layers with gate layers; and

forming first contact structures on the first staircase and second contact structures on the second staircase, the first contact structures being connected to the gate layers in the first section of the stack and the second contact structures being connected to the gate layers in the second section of the stack.

15. The method of claim 11, wherein the first section of the stack and the second section of the stack have a same number of gate layers.

16. The method of claim 12, wherein:

a height difference of two consecutive second group stair steps of the second group stair steps in the first direction is equal to the height of the N pairs of the gate layers and the insulating layers in the first section, and

a height difference of two consecutive second division stair steps of the second division stair steps in the first direction is equal to the height of the one pair of the gate layer and the insulating layer in the first section.

17. The method of claim 16, wherein corresponding group stair steps of the first group stair steps in the first staircase and the second group stair steps in the second staircase are of a same height.

18. The method of claim 14, wherein the removing the number of the sacrificial layers and the insulating layers of the second staircase further comprises:

removing the number of the sacrificial layers and the insulating layers that are of a same height as the first staircase.

19. The method of claim 14, further comprising:

shaping the sacrificial layers and the insulating layers to form stair steps in a third section of the stack corresponding to top select transistors of the channel structures.

20. The method of claim 16, wherein each first group stair step of the first group stair steps is formed of N first division stair steps and each second group stair step of the second group stair steps is formed of N second division stair steps.