

Asynchronous Transmission for NFC Card Emulation Mode

Field of the Invention

This invention relates to a method and system for asynchronous communication technique in Near Field Communication (NFC) system. Particularly, this invention relates to a method and system for generating a clock frequency that is close to the clock frequency received from the NFC reader for use in asynchronous communication technique in NFC system.

Summary of the Prior Art

Near Field Communication (NFC) enables contactless short range communication between two devices, typically requiring distance of 4 cm or less to initiate a connection. The connection can be done much faster than other communication technologies like Bluetooth or WiFi. The user only needs to bring two NFC supported devices closer and data will be transferred automatically. Some of its applications include credit card payment, ticketing, content sharing, quick pairing, and etc.

In general, NFC device requires very low power or no power for transmission when it operates in tag or card emulation mode. NFC tag/card device will first detect RF magnetic field from NFC reader device. The magnetic field energy is used to power the load component in the NFC tag/card device and transfer the data using passive load modulation (PLM). The term "passive" here is because there is no need for the NFC tag/card device to use its own energy for the transmission. Thus, when implemented in any mobile phones or tablet PCs, it still works when the battery dies and it does not affect device battery consumption.

Having good advantages, passive load modulation has its drawbacks. The amount of magnetic field that can be absorbed by the NFC tag/card device is limited to the antenna coupling between two NFC devices. Antenna coupling performance can deteriorate, for example, when smaller antenna is used or when two NFC devices are further apart.

Other NFC tag/card emulation technique is Active Load Modulation (ALM). This technique is getting popular as there is a strong interest in integrating NFC technology into mobile phones or tablet PCs. Mobile phones or tablet PCs have their own battery power, and thus, the NFC tag/card devices will be able to utilize their own battery power to generate the magnetic field during load modulation. ALM mode is also more suitable for smaller antenna implementation in the device and has better performance than the PLM mode. However, for

both PLM and ALM modes, normally clock recovery is required to ensure synchronous transmission between NFC devices.

A known NFC using analog phase-locked loop (PLL) to control ALM is disclosed in US 8934836 B2. Figure 1 shows the circuitry design of the NFC between two devices disclosed in US 8934836 B2.

The NFC Device 2 includes a clock recovery process 200 in the Analog module to recover the clock f_{R1} from NFC Device 1 magnetic field. The PLL is configured to receive one of the recovered clock and reference clock, and to utilize the received clock to control the active load modulation at both the digital receiver module and digital transmitter module. A driver is also used to adjust the amplitude of the voltage across the antenna. Since the clock recovery process is able to recover the clock f_{R1} from NFC Device 1 magnetic field, the transmission signal clock from NFC Device 2 can be exactly the same as f_{R1} . As a result, the NFC Device 1 will receive active load modulated signal from NFC Device 2 as conventional tag passive load modulated signal.

Unfortunately, US 8934836 B2 requires a complex analog RF front end with the clock recovery process 200 to recover the clock f_{R1} , and subsequently to use f_{R1} to control both the ALM reception and transmission. Further, the clock recovery process 200 and magnetic field generation may require the analog PLL forced in open loop state, which is difficult to implement in practice. Simpler or less complex of RF analog RF front end is desired for combo-chipset implementation where the size of analog RF front end could be limited.

In light of the above, those skilled in the art are striving to improve the clock recovery process for current NFC.

Summary of the Invention

The above and other problems are solved and an advance in the art is made by systems and methods provided by embodiments in accordance with the invention. A first advantage of embodiments of systems and methods in accordance with the invention is that there is no complex analog clock recovery in analog module since asynchronous transmission at different clock is adopted. A second advantage of embodiments of systems and methods in accordance with the invention is that NFC Reader/Poll Devices do not need to perform any clock offset adjustment to receive NFC Tag/Card Device signal generated at different clock frequency.

The above advantages are provided by embodiments of a system and a method in accordance with the invention operating in the following manner.

In accordance with embodiments of this invention, a method for an NFC card for use in asynchronous NFC card emulation mode transmission is provided. The method comprises estimating a carrier frequency offset between a carrier frequency of a NFC reader and a carrier frequency of the NFC card, adjusting digital baseband sampling of the baseband sample output at the NFC card emulation mode transmitter based on the estimated carrier frequency offset to obtain an adjusted baseband sample output, and modulating a RF transmitter based on the adjusted baseband sample output.

In accordance with embodiments of this invention, the step of estimating carrier frequency offset is triggered upon detecting a radio frequency (RF) magnetic field from the NFC reader.

In accordance with embodiments of this invention, the step of estimating carrier frequency offset is provided in the following manner. The method obtains an in-phase component (I) and a quadrature phase component (Q) for a number of samples of an input signal from an Analogue to Digital Converter (ADC) of the NFC card. The phase for each sample is then computed with the following expression: $\tan^{-1}(Q/I)$. Subsequently, the phase differences between a number of adjacent samples from the input signal are computed. These phase differences are then averaged to obtain the estimated carrier frequency offset which is in turn stored on a memory.

In accordance with embodiments of this invention, the step of obtaining the set of in-phase component (I) and quadrature phase component (Q) for the signal from the Analogue to Digital Converter (ADC) is provided in the following manner. The input signal at intermediate frequency is down-converted into a complex signal centered at zero frequency. Subsequently, a low pass filter is applied to filter harmonics components from the complex signal. The input signal at intermediate frequency into a complex signal centered at zero frequency is down-converted by multiplying the input signal with $\cos(2\pi f_c/f_s n)$ to obtain in-phase component (I) and multiplying the input signal with $\sin(2\pi f_c/f_s n)$ to obtain quadrature phase component (Q), wherein f_c is the carrier frequency, f_s is the ADC sampling frequency, and n is the sample number.

In accordance with embodiments of this invention, the step of adjusting digital baseband sampling of the baseband sample output at the NFC card emulation mode transmitter based on the estimated carrier frequency offset may be provided in the following manner. Input sample stream is received from a subcarrier generator. In response to receiving the input same stream, variables n , k and Acc are reset to zero. The estimated CFO is retrieved from the memory and the absolute of the estimated CFO is added to Acc . If the Acc is less than the input sampling frequency of the NFC card, the method outputs the input sample stream with the following expression $output[k]=input[n]$, where $output[k]$ is the output sample with reference to k , $input[n]$ is the input sample with reference to n . If there is any more input sample stream, the method increments n and k by 1 and repeats from the step of adding the absolute of the estimated CFO to Acc . If the Acc is more than the input sampling frequency of the NFC card, the method determines if the estimated CFO is greater than zero. If the estimated CFO is greater than zero, the method adds one sample and deducts the Acc by input sampling frequency. The method adds one sample by incrementing n by 1 and outputting the input sample with the following expression $output[k]=input[n]$. If the estimated CFO is less than zero, the method skips one sample and deducts the Acc by input sampling frequency. The method skips one sample by incrementing n by 1 and outputting the input sample with the following expression $output[k]=input[n]$.

In accordance with embodiments of this invention, the step of adjusting digital baseband sampling of the baseband sample output at the NFC card emulation mode transmitter based on the estimated carrier frequency offset may be provided in the following manner. Input sample stream is received from an encoder. In response to receiving the input sample stream from an encoder, the method sets Acc to zero and retrieves the estimated CFO from the memory. The absolute of the estimated CFO is added to Acc . If the Acc is less than the data-rate, the method establishes the number of samples for each encoded bit, N , is equal to number of samples per information bit, Bit_Len , where data-rate is equal to sampling frequency divided by Bit_Len . If the Acc is more than the data-rate, the method deducts the Acc by data-rate and determines if the estimated CFO is greater than zero. If the estimated CFO is greater than zero, the method establishes that N is equal to Bit_Len+1 . If the estimated CFO is less than zero, the method establishes that N is equal to Bit_Len-1 . The digital baseband sample for 1 bit duration is then generated based on value of N . If there is any more input sample stream, repeating from the step of adding the absolute of the estimated CFO to Acc .

In accordance with embodiments of this invention, a NFC card having a clock frequency offset (CFO) estimation module, a sample adjustment module and an analogue transmission module is provided to perform the method as described above.

Brief Description of the Drawings

The above advantages and features in accordance with this invention are described in the following detailed description and are shown in the following drawings:

Figure 1 illustrating a known circuitry design of the NFC between two devices;

Figure 2 illustrating an overview of an asynchronous transmission between two NFC devices in accordance with an embodiment of this invention;

Figure 3 illustrating an overview of a process flow performed by an NFC Device in card emulation mode upon detecting a carrier signal from another NFC Device in accordance with an embodiment of this invention;

Figure 4 illustrating a block diagram of the digital baseband of an NFC Device in asynchronous transmission in accordance with an embodiment of this invention;

Figure 5 illustrating a receiver processing timeline at the NFC Device in asynchronous card emulation mode in accordance with an embodiment of this invention;

Figure 6 illustrating a process flow performed by a CFO estimation module in accordance with an embodiment of this invention;

Figure 7 illustrating a block diagram of digital receiving module in accordance with an embodiment of this invention;

Figure 8 illustrating an embodiment of the CFO correction module in accordance with an embodiment of this invention;

Figure 9 illustrating a block diagram of digital transmission module for DBB controlled sample adjustment in accordance with an embodiment of this invention;

Figure 10 illustrating a process on the algorithm of DBB controlled sample adjustment at transmission mode shown in figure 9 in accordance with an embodiment of this invention;

Figure 11 illustrating a process on the algorithm of MAC controlled sample adjustment at transmission mode shown in figure 12 in accordance with an embodiment of this invention; and

Figure 12 illustrating a block diagram of digital transmission module for MAC controlled sample adjustment in accordance with an embodiment of this invention.

Detailed Description

This invention relates to a method and system for asynchronous communication technique in Near Field Communication (NFC) system. Particularly, this invention relates to a method and system for generating a clock frequency that is close to the clock frequency received from the NFC reader for use in asynchronous communication technique in NFC system.

A clock offset adjustment is introduced in NFC tag/card device for NFC transmission. This is different from conventional communication systems, such as cellular communications, WiFi or Bluetooth communications, where no clock offset adjustment is carried out at the transmission and the clock offset is typically taken care at the receiver.

In conventional NFC PLM communication, the NFC tag/card device recovers the clock from the NFC Reader/Poll Device magnetic field and uses this recovered clock to transmit the response frames back to the NFC Reader/Poll Device. So by nature of equal clock frequency, the NFC reader/poll device does not carry out any clock adjustment at the response frame reception.

With local power supply, NFC tag/card device may adopt ALM communication. However, the NFC reader/poll device has no idea whether the NFC tag/card device is in PLM or ALM mode. Further, the NFC reader/poll device may not carry out any clock adjustment at the response frame reception. Hence, NFC Tag/Card Device transmission at ALM mode should guarantee the clock of transmitted signal to be synchronized (both frequency and phase) with NFC reader/poll device clock.

In US 8934836 B2, the NFC tag/card device transmission employs the clock recovery process in Analog module to guarantee the clock of transmitted signal matches with NFC reader/poll device clock. In this invention, we introduce a sample-based low complexity method to compensate carrier frequency offset between NFC tag/card device and NFC reader/poll device, without the analog clock recovery process.

The required processes for asynchronous communication of NFC tag/card emulation mode will be described below.

Figure 2 illustrates the overview of an asynchronous transmission between two NFC devices. NFC Device 1 100 is a typical reader or poll device in NFC protocol with a clock frequency of f_{R1} . This means that the magnetic field generated by NFC device 1 100 is f_{R1} .

NFC Device 2 120 is an NFC tag/card or listen device in ALM mode. The NFC Device 2 102 employs a local clock generator 123 to generate the clock frequency of f_{R2} and supplies this clock to both digital receiver module 121 and digital transmission module 122, where f_{R2} may not be the same as f_{R1} . The local clock generator 123 is used as reference clock in all NFC card digital modules including Digital RX module and TX module.

Since f_{R2} is unlikely to be the same as f_{R1} , the digital receiver module 121 of NFC Device 2 120 is required to adjust the clock offset between f_{R1} and f_{R2} at the demodulation and decoding. Further details in this regard will be described below with reference to figure 5.

The digital transmission module 122 of NFC Device 2 120 employs a sample-based low complexity method to compensate carrier frequency offset between f_{R1} and f_{R2} . Further details pertaining to the sample-based low complexity method will be described below with reference to figure 5. As a result, the transmitted signal from NFC Device 2 120 is at the clock frequency of f_{R2} , which is approximated to f_{R1} but not exactly the same as f_{R1} . Thus, this is an asynchronous transmission to NFC Device 1 100.

For purposes of this discussion, an NFC tag/card device means the NFC device is in card emulation mode. The term 'tag' and 'card' can be used interchangeably.

Figure 3 illustrate an overview of a process flow 300 performed by NFC Device 2 120 upon detecting a carrier signal, f_{R1} , from NFC Device 1 100. The process flow 300 begins with 305 where NFC Device 2 120 detects a RF magnetic field from NFC Device 1 100. The signal received is processed in the analogue receiving module 124 in a conventional manner. Particularly, the signal is converted to digital signal by an Analogue to Digital Converter (ADC). For brevity, specific details pertaining to the analogue receiving module 124 are omitted.

In step 310, NFC Device 2 120 estimates the clock frequency offset (CFO), $\Delta f = f_{R1} - f_{R2}$, and stores the CFO information to a memory in the digital baseband. NFC Device 2 then continues to demodulate the received signal from NFC Device 1 in step 315. In step 320, process 300 determines whether NFC Device 2 120 is being switched to transmission state. If NFC Device 2 120 is still in receiving state, process 300 repeats step 315. In brief, the step 315 repeats until the NFC Device 2 is ready for transmission to NFC Device 1. If the NFC Device 2 120 is being switched to transmission state, process 300 proceeds to step 325. Further details regarding demodulating of the received signal will be described below with reference to figures 7 and 8.

In step 325, NFC Device 2 performs encoding and subcarrier generation of the information bit stream. In step 330, NFC Device 2 adjusts the digital baseband output samples based on the CFO estimation information stored on the memory. Further details regarding the adjustment of digital transmission sample will be described below with reference to figures 9-12. After the adjustment, the frequency of RF transmitted signal will be very close to f_{R1} and process 300 proceeds to step 335 to perform RF modulation by the analogue transmission module 125 in a conventional manner. For brevity, specific details pertaining to the analogue receiving module 124 are omitted. Process 300 ends after step 335.

Advantageously, NFC Device 1, which could be from a different manufacturer, does not need to perform any additional processing to receive the signal from NFC Device 2 since the f_{R2} is almost equal to f_{R1} .

In brief, the process for asynchronous NFC card emulation transmission comprises:

1. Estimating the carrier frequency offset (CFO) at the NFC card emulation mode receiver after RF field detection;
2. Storing the CFO information to the memory;
3. Adjusting digital sample of the baseband sample output at the NFC card emulation mode transmitter based on the CFO information;
4. Modulating the RF transmitter based on the adjusted baseband sample output.

An embodiment of this invention may include demodulation of the NFC reader signal after the carrier frequency offset estimation.

Figure 4 illustrates the overall block diagram of the digital baseband 400 of NFC Device 2 120 in asynchronous transmission. The digital baseband 400 of a NFC card emulation receiver comprises CFO estimation module 410, memory 420, digital receiving module 121 and the digital transmission module 122. The digital receiving module 121 converts the received signal into decoded bit stream using the carrier frequency offset from the memory 420. The digital transmission module 122 converts the input bit stream into baseband sampling output for RF modulation.

Figure 5 illustrates the receiver processing timeline at NFC Device 2 in asynchronous card emulation mode. AGC adjustment may be included before CFO estimation to ensure a stable receiving signal at the receiver. CFO estimation is performed during carrier wave (CW) period, which is available before receiving NFC Device 1 packet.

Further details regarding the CFO estimation module 410 will be described below with reference to figure 6. Further details regarding digital receiving module 121 and digital transmission module 122 will be described below with reference to figures 7-8 and 9-12 respectively.

Figure 6 illustrates a process flow 600 being performed by the CFO estimation module 410. The process 600 begins with step 605 by obtaining an in-phase component (I) and a quadrature phase component (Q) for a number of samples from the ADC output. The set of in-phase component (I) and quadrature phase component (Q) can be obtained in the following manner. First, the input signal (i.e. the ADC output) is down-converted at intermediate frequency into a complex signal centered at zero frequency. Particularly, the down-converting is by multiplying the input signal by locally generated down conversion sample of $\cos(2\pi f_c/f_s n)$ and $\sin(2\pi f_c/f_s n)$ to obtain the in-phase component (I) and quadrature component (Q) respectively, where f_c is the carrier frequency, f_s is the ADC sampling frequency, and n is the sample number. In this exemplary embodiment of invention, f_s is equal to 4 times of f_c . For $f_s = 4f_c$, the down conversion becomes very simple as the $\cos(2\pi f_c/f_s n)$ and $\sin(2\pi f_c/f_s n)$ can be replaced by the sequence of (1,0,-1,0) and (0,1,0,-1), respectively. Particularly, when $f_s = 4f_c$, $\cos(2\pi f_c/f_s n)$ would be equal to $\cos(\pi n/2)$. Substituting the sample number $n = 0,1,2,3,4,5,\dots$ into $\cos(\pi n/2)$, we get $\cos(0)$, $\cos(\pi/2)$, $\cos(\pi)$, $\cos(3\pi/2)$, $\cos(2\pi)$, $\cos(2.5\pi),\dots$ which would result in 1,0,-1,0,1,0,-1,0,1,0,... This is a repeated sequence of (1,0,-1,0).

Similarly for the sin function, when $f_s = 4f_c$, $\sin(2\pi f_c/f_s n) = \sin(\pi n/2)$. Substituting the sample number $n = 0,1,2,3,4,5,\dots$, we get $\sin(0)$, $\sin(\pi/2)$, $\sin(\pi)$, $\sin(3\pi/2)$, $\sin(2\pi)$, $\sin(2.5\pi),\dots$ which would result in 0,1,0,-1,0,1,0,-1,0,1,0,-1,... This is a repeated sequence of (0,1,0,-1).

After down-converting the input signal, a low pass filtering is applied to filter away harmonics components from the input signal. Alternatively, Coordinate Rotation Digital Computer (CORDIC) algorithm may be used to obtain the in-phase component (I) and quadrature phase component (Q) without departing from the invention.

In step 615, the phase of the vector from the complex signal output which consists of in-phase component (I) and quadrature phase component (Q) is computed using the following expression, $\text{phase} = \tan^{-1}(Q/I)$ for each sample. Essentially, the arctan of Q/I provides the phase shift of the vector of Q/I .

In step 620, the process 600 computes the phase differences between two adjacent samples, i.e. at $t=i$ and $t=(i+1)$ where $i=1,2,3,\dots$. In step 625, the CFO estimate is then

obtained from the average of the phase differences between two adjacent samples. The estimated CFO is then stored on the memory in step 630. Process 600 ends after step 630.

Figure 7 illustrates a block diagram of digital receiving module 121. The digital receiving module 121 comprises a CFO correction module 710 to compensate the asynchronous frequency component, an envelope/phase detector 720 to detect the envelope/phase component of complex baseband signal, and a DEC module 730 to obtain the decoded bit stream. The envelope/phase detector 720 or SYNC process may include DC cancellation to remove the DC component of the signal. Further, the envelope detector can be implemented by using simple approximation of the square root function. When high precision envelope/phase detector is used, CFO correction module 710 may not be required and can be replaced by a simple down conversion based on zero frequency offset.

Figure 8 illustrates an exemplary embodiment of the CFO correction module 710. The CFO correction module 710 may consist of phase rotation module 712, a low pass filter 714 and a decimate module 716. The phase rotation is based on frequency offset information. The rotation is equivalent to multiplying the input with locally generated down conversion sample of $\cos(2\pi(f_c + \Delta f)/f_s n)$ and $\sin(2\pi(f_c + \Delta f)/f_s n)$ where Δf is carrier frequency offset. The LPF 714 filters the phase rotation output. The decimate module 716 decimates the CFO filter output to lower sampling rate.

Figure 9 illustrates a block diagram of digital transmission module 122. The digital transmission module 122 comprises an encoder 910, a subcarrier generator 920 and a sample adjustment module 930. The information bit stream is fed to the encoder 910 and subcarrier generator 920. The output of subcarrier generator is the digital baseband output of NFC Device 2 in synchronous card emulation mode. A digital transmission sample adjustment module 930 is provided to adjust the digital baseband output to compensate the carrier frequency offset. The sample adjustment module 930 can be based on either digital baseband (DBB) or medium access control (MAC). The block diagram shown in figure 9 is based on DBB controlled sample adjustment. Further details for sample adjustment module in accordance with MAC will be described below with reference to figures 11 and 12. The estimated CFO is retrieved back from the memory 420 during transmission process. The output of digital transmission sample adjustment module 930 is sent to RF module for RF modulation.

For purposes of this discussion, the Digital transmission sample adjustment module 930 is applicable for all NFC specifications, e.g. ISO14443A, ISO14443B, FeliCa, and ISO15693, with any data rates.

DBB controlled sample adjustment

Figure 10 illustrates a process 1000 on the algorithm of DBB controlled sample adjustment at transmission mode shown in figure 9.

The “input sample” is the output from subcarrier generator 920 in Figure 9. In brief, the samples are adjusted whenever the accumulation of the absolute value of estimated CFO (i.e. Acc) is greater than or equal to the input sampling frequency (i.e. Sampling_freq). Input sampling frequency could be 13.56MHz. 1 sample is added if the value of estimated CFO is positive, and 1 sample is skipped if the value of the estimated CFO is negative.

Process 1000 begins with step 1005 by receiving input sample stream from the output of subcarrier generator 920 in Figure 9. In step 1010, process 1000 resets n, k and Acc to zero where n, k and Acc are variables. Variables n and k are used to indicate the input sample number and output sample number respectively while variable Acc refers to the accumulated estimated CFO.

In step 1015, process 1000 adds the absolute of estimated CFO to Acc. If the Acc is determined to be more than the input sampling frequency in step 1020, process 1000 proceeds to step 1030. If the Acc is determined to be less than the input sampling frequency in step 1020, process 1000 proceeds to step 1025.

In step 1025, the input sample stream is directly output since the accumulated estimated CFO is not more than the input sampling frequency.

In step 1030, process 1000 determines whether the estimated CFO is greater than zero, i.e. whether the estimated CFO is positive or negative. If the estimated CFO is positive, process 1000 proceeds to step 1040. If the estimated CFO is negative, process 1000 proceeds to step 1034. A positive estimated CFO means that f_{R1} is greater than the input sampling frequency and an additional sample is added. A negative estimated CFO means that f_{R1} is smaller than the input sampling frequency and one input sample is skipped.

In step 1034, process 1000 increases n by 1 and subsequently outputs the next input sample with the following expression $output[k]=input[n]$ in step 1036. This is so that the current input sample is skipped and the next input sample is being outputted.

In step 1040, process 1000 outputs the input sample with the following expression $output[k]=input[n]$. In step 1044, process 1000 increase k by 1 and subsequently outputs the input sample with the following expression $output[k]=input[n]$ in step 1046. This is so that the same sample is outputted twice.

For purpose of this discussion, the expression $\text{output}[k] = \text{input}[n]$ is used to illustrate which input sample is being outputted by the sample adjustment module 930.

In step 1050, process 1000 deducts the Acc by input sampling frequency. In step 1055, process 1000 determines whether there is any more input sample stream. If there is more input sample stream, process 1000 proceeds to step 1060 to increment n and k by 1 and subsequently repeats from step 1015. If there is no more input sample stream, process 1000 ends.

MAC Controlled TX sample adjustment

The use of RTL, which is software defined, may have limitation to implement DBB controlled TX sample adjustment as the number of samples for each information bit is given by MAC. Thus, for the implementation of sample adjustment, MAC may provide the value of N , i.e. number of samples for each encoded bit. The value of N is adjusted based on the estimated CFO. Figure 12 illustrates the block diagram for sample adjustment module in accordance with MAC. The sample adjustment module 940 receives the encoded bit stream from the encoder 910 and implements transmission sample adjustment to determine the value of N for each encoded bit. The value of N together with the encoded bit stream is then forwarded to subcarrier generator 920. The subcarrier generator 920 then generates DBB samples for RF modulation.

As an example, for data rate = 106kbps, the default value of N is 128, which is obtained from the ratio between sampling rate of 13.56MHz and data rate of 106kbps under synchronous condition. The sample adjustment module 940 outputs the value of N for each encoded bit back to the subcarrier generator 920. For data rate = 106kbps, the value of N is 129 if 1 more sample is added, 127 if 1 sample is removed, or 128 if the default value is chosen.

Similar to DBB sample adjustment, Acc is the accumulation of estimated CFO which is obtained from memory 420. Bit_len is the number of samples per information bit. For example, if data-rate = 106kbps, Bit_len = 128; if data-rate = 212kbps, Bit_len = 64; etc. The value of N will be equal to Bit_len if $\text{Acc} \leq \text{data-rate}$. When $\text{Acc} > \text{data-rate}$, N will be equal to Bit_len+1 or Bit_len-1 depending on the sign of estimated CFO. DBB samples for 1 bit duration are generated based on the value of N . The relationship between data-rate, Bit_Len and sampling frequency is shown in table 1 below.

Data-rate (kbps)	Sampling frequency	Bit_Len
106	13.568Mhz	128

212		64
424		32
848		16

Figure 11 illustrates a process 1100 on the algorithm of MAC controlled sample adjustment at transmission mode shown in figure 12. Process 1100 begins with step 1105 by receiving encoded bit stream from the encoder 910 in Figure 12. In step 1110, process 1100 resets Acc to zero.

In step 1115, process 1100 adds the absolute of CFO estimated offset frequency to Acc. If the Acc is determined to be more than the data-rate in step 1120, process 1100 proceeds to step 1125. If the Acc is determined to be less than the data-rate in step 1120, process 1100 proceeds to step 1140.

In step 1140, the number of samples for each encoded bit is equal to Bit_Len since the accumulated estimated CFO is not more than the data-rate. The value of N is transmitted to the subcarrier generator 920.

In step 1125, process 1100 deducts the Acc by the relevant data-rate.

In step 1130, process 1100 determines whether the estimated CFO is greater than zero, i.e. whether the estimated CFO is positive or negative. If the estimated CFO is positive, process 1100 proceeds to step 1135. If the estimated CFO is negative, process 1100 proceeds to step 1145. A positive estimated CFO means that f_{R1} is greater than the input sampling frequency and an additional sample is added in step 1135. A negative estimated CFO means that f_{R1} is smaller than the input sampling frequency and one sample is removed in step 1145. The value of N is then transmitted to the subcarrier generator 920.

In step 1150, the digital baseband sample for 1 bit duration based on value of N is generated by the subcarrier generator 920.

In step 1155, process 1100 determines whether there is any more input sample stream. If there is more input sample stream, process 1100 repeats from step 1115. If there is no more input sample stream, process 1100 ends.

A wireless communication device may include both NFC in ALM and PLM modes. During the ALM mode, the asynchronous card emulation mode as illustrated above will be implemented. During the PLM mode, it will use conventional system to recover the clock from the magnetic field. Hence, the asynchronous card emulation mode as illustrated above

can be implemented to existing wireless communication device including both NFC in ALM and PLM modes.

The above is a description of embodiments of an NFC device in accordance with the present invention. It is foreseeable that those skilled in the art can and will design alternative NFC devices based on this disclosure that infringe upon this invention as set forth in the following claims.

CLAIMS:

1. A method for a Near Field Communication (NFC) card for use in asynchronous NFC card emulation mode transmission comprising:
 - estimating a carrier frequency offset (CFO) between a carrier frequency of a NFC reader and a carrier frequency of the NFC card;
 - adjusting digital baseband sampling of a baseband sample output at a NFC card emulation mode transmitter in the NFC card based on the estimated carrier frequency offset to obtain an adjusted baseband sample output; and
 - modulating a radio frequency (RF) transmitter in the NFC card emulation mode transmitter based on the adjusted baseband sample output.
2. The method according to claim 1, wherein the step of estimating the carrier frequency offset is triggered upon detecting a RF magnetic field from the NFC reader.
3. The method according to claim 1, wherein the step of estimating the carrier frequency offset comprises:
 - obtaining an in-phase component (I) and a quadrature phase component (Q) for a plurality of samples of an input signal from an Analogue to Digital Converter (ADC) of the NFC card;
 - computing a phase for each sample;
 - computing phase differences between a plurality of adjacent samples from the input signal;
 - averaging the phase differences to obtain the estimated carrier frequency offset; and
 - storing the estimated carrier frequency offset in a memory in the NFC card.
4. The method according to claim 3, wherein the step of obtaining the set of in-phase component (I) and quadrature phase component (Q) for the signal from the Analogue to Digital Converter (ADC) comprises:
 - down-converting the input signal at an intermediate frequency into a complex signal centered at zero frequency; and
 - applying a low pass filter for the complex signal to filter harmonics components from the complex signal.
5. The method according to claim 4, wherein the step of down-converting the input signal at the intermediate frequency into the complex signal centered at zero frequency comprises:

multiplying the input signal with $\cos(2\pi f_c/f_s n)$ to obtain in-phase component (I); and multiplying the input signal with $\sin(2\pi f_c/f_s n)$ to obtain quadrature phase component (Q), wherein f_c is the carrier frequency, f_s is an ADC sampling frequency, and n is a sample number.

6. The method according to claim 3, wherein the phase for each sample is computed with the following expression: $\tan^{-1}(Q/I)$.

7. The method according to any one of claims 1 to 6, wherein the step of adjusting the digital baseband sampling of the baseband sample output at the NFC card emulation mode transmitter based on the estimated carrier frequency offset comprises:

receiving input sample stream from a subcarrier generator;
 setting n , k and Acc to zero;
 retrieving the estimated CFO from the memory;
 adding the absolute of the estimated CFO to Acc ;
 determining if the Acc is more than the input sampling frequency of the NFC card;
 outputting the input sample stream with the following expression $output[k]=input[n]$, in response to the Acc being determined to be less than the input sampling frequency;
 determining if there is any more input sample stream; and
 incrementing n and k by 1 and repeating from the step of adding the absolute of the estimated CFO to Acc in response to determining that there is more input sample stream, wherein n and k are variables, $output[k]$ is an output sample number, $input[n]$ is an input sample number, and Acc is an accumulation of estimated CFO.

8. The method according to claim 7, wherein the step of adjusting the digital baseband sampling of the baseband sample output at the NFC card emulation mode transmitter based on the estimated carrier frequency offset further comprises:

determining if the estimated CFO is greater than zero;
 skipping a sample in response to determining the estimated CFO is less than zero;
 adding a sample in response to determining the estimated CFO is greater than zero;
 and
 deducting the Acc by the input sampling frequency.

9. The method according to claim 8, wherein the step of skipping a sample comprises:
 incrementing n by 1; and
 outputting the input sample stream with the following expression $output[k]=input[n]$.

10. The method according to claim 8, wherein the step of adding a sample comprises:
 - outputting the input sample stream with the following expression $\text{output}[k]=\text{input}[n]$;
 - increment k by 1; and
 - outputting the input sample stream with the following expression $\text{output}[k]=\text{input}[n]$.

11. The method according to any one of claims 1 to 6, wherein the step of adjusting the digital baseband sampling of the baseband sample output at the NFC card emulation mode transmitter based on the estimated carrier frequency offset comprises:
 - receiving encoded bit stream from an encoder;
 - setting Acc to zero;
 - retrieving the estimated CFO from the memory;
 - adding the absolute of the estimated CFO to Acc ;
 - determining if the Acc is more than a data-rate,
 - establishing the number of samples for each encoded bit, N , which is equal to number of samples per information bit, Bit_Len , in response to the Acc being less than the data-rate;
 - generating the digital baseband sample for 1 bit duration based on a value of N ;
 - determining if there is any more input sample stream; and
 - repeating from the step of adding the absolute of the estimated CFO to the Acc in response to determining that there is more input sample stream, wherein the data-rate is equal to a sampling frequency divided by Bit_Len , and Acc is the accumulation of estimated CFO.

12. The method according to claim 11 where the step of adjusting the digital baseband sampling of the baseband sample output at the NFC card emulation mode transmitter based on the estimated carrier frequency offset further comprises:
 - deducting the Acc by the data-rate in response to the Acc being determined to be more than the data-rate;
 - determining if the estimated offset frequency is greater than zero;
 - establishing N is equal to $\text{Bit_Len}+1$ in response to the estimated CFO is greater than zero; and
 - establishing N is equal to $\text{Bit_Len}-1$ in response to the estimated CFO is less than zero.

13. A Near Field Communication (NFC) card comprising:
 - a clock frequency offset (CFO) estimation module configured to estimate a carrier frequency offset between a carrier frequency of a NFC reader and a carrier frequency of

the NFC card;

a sample adjustment module configured to adjust digital baseband sampling of a baseband sample output at a transmitter of the NFC card based on the estimated carrier frequency offset to obtain an adjusted baseband sample output; and

an analogue transmission module configured to modulate a radio frequency (RF) transmitter in the NFC card based on the adjusted baseband sample output.

14. The NFC card according to claim 13, wherein the CFO estimation module is triggered to estimate the carrier frequency offset upon detecting a RF magnetic field from the NFC reader.

15. The NFC card according to claim 14, wherein the CFO estimation module is configured to:

obtain an in-phase component (I) and a quadrature phase component (Q) for a plurality of samples of an input signal from an Analogue to Digital Converter (ADC) of the NFC card;

compute a phase for each sample;

compute phase differences between a plurality of adjacent samples from the input signal;

average the phase differences to obtain the estimated carrier frequency offset; and

store the estimated carrier frequency offset in a memory in the NFC card.

16. The NFC card according to claim 15, wherein the CFO estimation module is further configured to:

down-convert the input signal at an intermediate frequency into a complex signal centered at zero frequency; and

apply a low pass filter for the complex signal to filter harmonics components from the complex signal.

17. The NFC card according to claim 16 wherein the CFO estimation module is further configured to:

multiply the input signal with $\cos(2\pi f_c/f_s n)$ to obtain in-phase component (I); and

multiply the input signal with $\sin(2\pi f_c/f_s n)$ to obtain quadrature phase component (Q) wherein f_c is the carrier frequency, f_s is an ADC sampling frequency, and n is a sample number.

18. The NFC card according to claim 15 wherein the phase for each sample is computed

with the following expression: $\tan^{-1}(Q/I)$.

19. The NFC card according to any one of claims 13 to 18 wherein the sample adjustment module is configured to:

- receive input sample stream from a subcarrier generator;
- set n, k and Acc to zero;
- retrieve the estimated CFO from the memory;
- add the absolute of the estimated CFO to Acc;
- determine if the Acc is more than the input sampling frequency of the NFC card;
- output the input sample stream with the following expression $\text{output}[k]=\text{input}[n]$, in response to the Acc being determined to be less than the input sampling frequency;
- determine if there is any more input sample stream; and
- increment n and k by 1 and repeat from the step of adding the absolute of the estimated CFO to Acc in response to determining that there is more input sample stream, wherein n and k are variables, $\text{output}[k]$ is an output sample number, $\text{input}[n]$ is an input sample number, and Acc is an accumulation of estimated CFO.

20. The NFC card according to claim 19 wherein the sample adjustment module is further configured to:

- determine if the estimated CFO is greater than zero;
- skip a sample in response to determining the estimated CFO is less than zero;
- add a sample in response to determining the estimated CFO is greater than zero;
- and
- deduct the Acc by the input sampling frequency.

21. The NFC card according to claim 20 wherein the sample adjustment module is further configured to skip a sample by:

- incrementing n by 1; and
- outputting the input sample stream with the following expression $\text{output}[k]=\text{input}[n]$.

22. The NFC card according to claim 20 wherein the sample adjustment module is further configured to add a sample by:

- outputting the input sample stream with the following expression $\text{output}[k]=\text{input}[n]$;
- incrementing k by 1; and
- outputting the input sample stream with the following expression $\text{output}[k]=\text{input}[n]$.

23. The NFC card according to any one of claims 13 to 18 wherein the sample

adjustment module is configured to:

- receive encoded bit stream from an encoder;
- set Acc to zero;
- retrieve estimated CFO from the memory;
- add the absolute of the estimated CFO to Acc;
- determine if the Acc is more than a data-rate,
- establish the number of samples for each encoded bit, N, is equal to number of samples per information bit, Bit_Len, in response to Acc being less than the data-rate;
- generate the digital baseband sample for 1 bit duration based on value of N;
- determine if there is any more input sample stream; and
- repeat from the step of adding the absolute of the estimated CFO to the Acc in response to determining that there is more input sample stream, wherein data-rate is equal to sampling frequency divided by Bit_Len.

24. The NFC card according to claim 23 where the sample adjustment module is further configured to:

- deduct the Acc by data-rate in response to the Acc being determined to be more than data-rate;
- determine if the estimated offset frequency is greater than zero;
- establish N is equal to Bit_Len+1 in response to the estimated CFO is greater than zero; and
- establish N is equal to Bit_Len-1 in response to the estimated CFO is less than zero.