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Semiconductor Drive Circuit

This invention relates to a drive circuit for a three
5 electrical contact semiconductor that ensures optimum turn-on
and turn-off time rates for the semiconductor.

Our copending Patent Application No. 2082002 discloses
a drive circuit coupled to electrical devices connected
in parallel in a circuit network, which circuit ensures
10 that the individual on-times of the respective
electrical devices are mutually identical as regards
turn-on times, turn-off times and total on-time periods.

It has been long recognized that when high power levels
are sought to be transmitted through a transistorized
15 circuit and the power rating of individual transistors
available for use in such a circuit is insufficient,
then high power operation can be obtained by the
parallel connection and operation of lower power rated
transistors. The employment of transistors in parallel
20 in such circuits is not without problems. The problems
are varied and a number of these problems have been
recognized and apparently successfully treated. Inverter
circuits provide a typical setting where transistors
are operated in parallel and from time-to-time due to
25 excessive current through the transistors, the transistors
burnout.

Historically, these inverter circuits have been provided with excess current protective circuits.

Transistors in these circuits must be carefully matched, otherwise one of the transistors will take over the whole load of the output current and be destroyed.

US Patent No. 3,056,094 (Crawford) recognizes this matching problem and provides a solution that provides balanced current through a number of transistors connected in parallel to a load. The balance is

achieved by connecting a resistor in series with the base electrode of each transistor. The value of each of these resistors independently controls the base current for its associated transistor. This

independent control enables the base bias currents of each of the transistors to be adjusted so that each transistor contributes substantially equally to the output load current even though the transistors used are not matched. The Crawford patent therefore recognizes the steady state power handling capability

of a number of unmatched transistors operated in parallel, but does not recognize that the turn-on and turn-off times of the transistors may differ and that the transistor may burnout should a single transistor turn completely on before another. Similarly a transistor may burnout if a transistor turns completely off before another. The invention to be described hereinafter

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recognizes the turn-on and turn-off problem and provides enhanced turn-on and turn-off rates for a semiconductor, enabling the burnout problem during such periods to be controlled.

5 US Patent No. 4,099,255 (Nygaard) also recognizes the need for a current protective circuit for an inverter with semiconductor control elements. The Nygaard invention is based on the discovery that burnout of semiconductor control elements in circuits that employ
10 an excess current protective circuit is tied to the fact that discharge currents in filter condensers in the control circuit are the culprit involved in transistor burnout. The Nygaard patent, not unlike the Crawford patent noted above, concerns itself with current detection
15 and control while the invention to which our Patent Application 2082002 is directed recognizes that the excess current problem may be resolved if the transistors operated in parallel can be exactly matched in respect of their total on-time where the total on-time includes a
20 matching of turn-on and turn-off times for the transistors.

All of the above attempts to provide excess current protective circuits, including that of our British Patent Application No. 2082002, would be enhanced by improving the turn-on and turn-off rates of the
25 semiconductors.

According to the invention, there is provided a drive circuit for a three electrical contact semiconductor in a circuit having a power source connected to a first electrical contact of the semiconductor and a load connected to a third electrical contact of the semiconductor. The drive circuit includes a logic signal source. A positive feedback circuit is electrically coupled between the first electrical contact and a second electrical contact of the semiconductor.

5 A resonant, impulse current turn-on circuit is coupled to the second electrical contact and is controlled by the logic signal source. A resonant, impulse current turn-off circuit is coupled to the second electrical contact and is controlled by the logic signal source.

10 A fixed current level turn-on circuit is optionally also coupled to the second electrical contact and is controlled by the logic signal source. A turn-off steady state reverse bias circuit is optionally also coupled to the second electrical contact and is

15 controlled by the logic signal source. The foregoing drive circuit particularly rapid turn-on and turn-off time rates for the semi-conductor.

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DRAWINGS:

Figure 1 depicts a drive circuit embodying the invention;

25 Figure 1a is an illustration of a series resonant turn-on circuit found in Figure 1,

Figure 1b is an illustration of a series resonant turn-off circuit found in Figure 1,

Figure 2 is a signal timing chart that illustrates the signals present in the circuit of Figure 1, and

5 Figure 3 illustrates how the drive circuit arrangement of Figure 1 may be employed in a parallel transistor arrangement.

Reference is first made to Figure 1 which depicts an embodiment of a drive circuit embodying the invention.

10 The drive circuit includes a three electrical contact semiconductor in the form of transistor Q'_1 , in a circuit having a power source delivered across terminals 161 across positive terminal 161 and negative terminal 162, and a second semiconductor in the form of transistor
15 Q'_2 , as shown in dotted outline connected in parallel to transistor Q'_1 . Power delivered across positive and negative terminals 161, 162 is delivered to a load 166. The power source is connected to a first electrical contact 163 of transistor Q'_1 and a third electrical
20 contact 164 of transistor Q'_1 via leads 167, 168, positive feedback transformer winding 169 and lead 170 to first electrical contact 163. The first electrical contact 163 is electrically coupled to a second electrical contact 165 of the transistor base Q'_1 and
25 the third electrical contact 164 is coupled to the base of transistor Q'_1 and electrically connected to leads 171, 172 and 173 to the load 166, which load 166 is

electrically connected in turn to the negative power terminal 162. The drive circuit of Figure 1 includes the following basic components: a logic signal source 178 shown in dotted outline at the left hand end of Figure 1. The logic signal source 178 is electrically connected to a transformer coupled drive circuit 179 shown in dotted outline at the centre of Figure 1, by electrical leads 181, 182, 183 and 184.

The transformer coupled drive circuit 179 includes a positive feedback circuit electrically coupled between the first electrical contact 163 and the second electrical contact 165 of the transistor Q'_1 . This positive feedback circuit is provided through transformer winding N5 for reasons that will become apparent and be explained more fully hereinafter. The transformer winding N5 bears the additional designation of reference numeral 169. This positive feedback through the winding N5 will provide for better efficiency at partload.

A resonant impulse current turn-on signal circuit 186 shown in dotted outline is coupled through transformer winding N3 to the second electrical contact 165 and is controlled by the logic signal source 178. The details of the resonant impulse turn-on signal circuit 186 are set forth in Figure 1a and will be explained more fully hereinafter.

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A resonant impluse current turn-off signal circuit 187 shown in dotted outline provides an impluse turn-off signal through winding N4 of a value greater than the turn-on pulse to provide effective rapid turn-off and overcome the positive feedback portion of the base current to transistor Q'_1 . The resonant impluse current turn-off signal 187 is coupled through winding N4 to the second electrical contact 165 and is controlled by the logic signal source 178 in a manner to be described more fully hereinafter, when Figure 1b is described.

A fixed current level turn-on circuit is provided by a path from a 28 VDC source through leads 188, 189, transformer winding N2, lead 191, transistor diode combination Q_B , D_2 , and lead 192 to ground 193. This fixed current level turn-on circuit is coupled via windings N2 and N6 through resistor R3 to the second electrical contact 165 of the base Q'_1 .

The final component of the drive circuit is a turn-off steady state reversed bias circuit that is provided by a path through windings N1, transistor Q_A for the steady state turn-off and reverse bias of transistor Q'_1 . The drive circuit broadly described above provides

improved turn-on and turn-off rates for the transistor Q'_1 .

Reference is now made to Figure 2 which is a signal timing chart that illustrates the signals present in the circuit of Figure 1. At line J of Figure 2 there is illustrated the desired ideal Q' base current waveform. From the description in British Patent Specification No. 2082002 in respect of the turn-on, turn-off problem, it should be recognized that in order to insure consistent definitive turn-on and turn-off times, the base current during the turn-on and turn-off times should be overdriven in order that the most rapid turn-on and turn-off occurs. Accordingly, at line J of Figure 2 there is shown a positive overdrive turn-on square wave pulse 196 and a negative overdrive turn-off pulse 197. The drive circuit of Figure 1 is intended to provide a close approximation of the desired Q'_1 base current shown in line J of Figure 2. The resultant waveform of a Q'_1 base current provided by the drive circuit is shown on line L of Figure 2. The positive overdrive turn-on signal provided to the base of Q'_1 as shown at line L of Figure 2 is indicated by the reference numeral 198. The series resonant turn-on circuit 186 of Figure 1a provides the waveform 198.

The series resonant turn-off circuit 187 of Figure 1b provides the negative overdrive pulse 199 as shown at line L of Figure 2. Reference is again made to Figure 1 in which there is shown a trigger signal source 178 via lead 177. The logic network illustrated in the logic signal source 178 illustrates an example of how the required logic signals that are essential to control the transformer coupled drive 179 can be generated. Returning to Figure 2 the signal curve 31 illustrated on line A appears on lead 177 of Figure 1. This is the same type of signal described with respect to Figures 2, 3, 5, 7 and 9 of British Patent Specification No. 2082002. The signal present on lead 183 is shown at line F. The signal present on lead 181 is shown by the curve illustrated on line G. The signal present on lead 182 is shown by the signal illustrated on line H, and finally, the signal present on lead 184 is shown by the signal present on line I. The envelope of the signal shown at line L of Figure 2 is made up of 4 separate and simultaneously provided signal portions. The current level represented by the curve 202 is a function of the number of turns of transformer winding N_2 , while the curve 203 is a function of the ratio of the transformer windings N_5 to N_6 , times the collector current I_C of the transistor Q'_1 plus the current level represented by curve 202. The positive overdrive turn-on current

curve 198 is accomplished by the series resonant turn-on circuit of Figure 1a. The series resonant turn-off circuit of Figure 1b provides the fourth and final component of Q'_1 base current shown at line L of Figure

5 2. The fundamental laws of series resonant circuits are well known, so that no further explanation of the circuits of Figures 1a and 1b is necessary. It is sufficient to note, with respect to Figures 1a and 1b, as well as Figure 1, that the resonant impulse
10 turn-on signal circuit through the winding N3 required to speed up the turn-on is accomplished by the resonant combination of capacitors C_1 with the inductance L_t of the transformer T_1 . The turn-off pulse 199 is achieved by the combination of capacitor C_2 with the inductance
15 L_t of the transformer T_1 . Charging of the capacitors C_1 and C_2 is provided by resistors R_1 and R_2 respectively, while diodes D_3 and D_4 provide for stopping the resonant conduction after the first half cycle.

Reference is now made to Figure 3 which shows in block
20 diagram form how the drive circuits of Figure 1 may be employed in a parallel transistor Q'_1 and Q'_2 arrangement of the kind described and claimed in British Patent Specification 2082002.

In Figure 1 transistor Q'_2 was shown in broken line
25 fashion. In the brief description of Figure 3 the same reference numerals used in Figure 1 will be

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employed to designate the same components. Accordingly,
a source of power is provided across positive and
negative terminals 161 and 162. A trigger signal
source 23 is shown electrically connected in parallel
5 to logic signal source 178 and 178a via leads 177,
177a and 177b. The logic signal source 178 is
electrically coupled to the transformer coupled drive
circuit 179 via leads 181, 182, 183 and 184. In a
similar fashion logic signal source 178a is electrically
10 coupled to the transformer coupled drive circuit
179a via electrical leads 181a, 182a, 183a and 184a.
Transformers T_1 and T_2 respectively couple the
aforementioned drive circuits 179, 179a to transistors
 Q'_1 and Q'_2 as shown. The load 166 is provided with
15 power through parallel connected transistors Q'_1 , Q'_2 .

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CLAIMS

1. A drive circuit for a three electrical contact semiconductor in a circuit having a power source connected to a first electrical contact of the semiconductor and a load connected to a third electrical contact of the semiconductor, which drive circuit includes in combination;
5 a logic signal source,
a positive feedback circuit electrically coupled between the first electrical contact and a second electrical contact of the semiconductor,
10 a resonant, impulse current turn-on circuit coupled to the second electrical contact and controlled by the logic signal source, and
a resonant, impulse current turn-off circuit
15 coupled to the second electrical contact and controlled by the logic signal source.
2. A drive circuit according to claim 1, wherein there is in addition a fixed current level turn-on circuit
20 coupled to the second electrical contact and controlled by the logic signal source.
3. A drive circuit according to claim 2, wherein the resonant, impulse current turn-on circuit provides an overdrive
25 turn-on pulse the peak amplitude of which is significantly greater than that of the current provided by the fixed current level turn-on circuit; and the resonant, impulse current turn-off circuit provides an overdrive turn-off pulse the peak amplitude of which exceeds that of the
30 overdrive turn-on pulse.
4. A drive circuit according to any preceding claim, wherein there is in addition a turn-off steady



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state reverse bias circuit coupled to the second electrical contact and controlled by the logic signal source.

5. A drive circuit according to any preceding claim, wherein the semiconductor is a transistor and the first, second and third electrical contacts are respectively an emitter, a base and a collector.

6. A drive circuit according to claim 5, wherein the positive feedback circuit includes a transformer which couples the emitter and the base thereby to provide better efficiency at part load.

7. A drive circuit having the features of claims 1 to 6 inclusive, wherein the resonant, impulse current turn-on circuit, the resonant, impulse current turn-off circuit, the fixed current level turn-on circuit and the turn-off steady state reverse bias circuit are all inductively coupled through the transformer to the base of the transistor.

8. A drive circuit according to claim 7, wherein the resonant impulse current turn-on circuit includes a winding inductively coupled to the transformer and a capacitor that cooperates in a resonant manner with the inductance of the transformer to speed up the turn-on.

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9. A drive circuit according to claim 8, wherein the resonant, impulse current turn-off circuit includes a winding inductively coupled to the transformer, and a capacitor that cooperates in a resonant manner with the inductance of said transformer to provide an impulse current turn-off having a greater value than the impulse current turn-on.
10. A drive circuit substantially as described herein with reference to the drawings.
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