SUPERIOR INTEGRITY OF HIGH-K METAL GATE STACKS BY CAPPING STI REGIONS

ABSTRACT

When forming high-k metal gate electrode structures in an early manufacturing stage integrity of an encapsulation and thus integrity of sensitive gate materials may be improved by reducing the surface topography of the isolation regions. To this end, a dielectric cap layer of superior etch resistivity is provided in combination with the conventional silicon dioxide material.

Fig 2j