Silicon Oxycarbide and Silicon Carbonitride Based Materials for MOS Devices

[0001] This applications claims priority to provisional patent application serial number 60/565,630, filed April 27, 2004, and entitled "Silicon Oxycarbide and Silicon Carbonitride Based Materials for MOS Devices," which application is incorporated herein by reference.

FIELD OF INVENTION

[0002] This invention relates generally to semiconductor devices, and more specifically to contact etch stop layers.

BACKGROUND

[0003] In deep sub micron microelectronic manufacturing, silicon nitride films are widely employed as stop layers during contact etching. As is well known in the art, the inter-level dielectric (ILD) is formed to provide insulation between the MOS devices and overlying metal lines that will be formed subsequently. The contact openings are made through the ILD layer to the source, drain and gate. The ILD layer is relatively thick, and it is hard to control the etching process in order to not over etch. The contact etch stop layer is formed prior to the formation of the ILD layer. A first highly selective etching is conducted to etch the ILD layer and stop at the etch stop layer. A second selective etching is conducted to etch the stop layer so that the underlying layer is exposed.

[0004] The conventionally used silicon nitride etch stop layer has several disadvantages. It has a high dielectric constant value (also known as k value), typically about 7.5 to 8. The high k value increases high parasitic capacitance, which degrades the device performance. Additionally,

the deposition rate of the silicon nitride film is low and the deposition temperature is high, which are not desirable process characteristics.

SUMMARY OF THE INVENTION

[0005] The preferred embodiments of the present invention use silicon oxycarbide (SiCO) (also called Silicon, Carbon containing based oxide) and silicon carbonitride (SiCN) (also called Silicon, Carbon containing based nitride) based materials, such as carbon doped oxide (CDO) and nitride doped silicon carbide (NDC) to make the contact etch stop layer.

[0006] The SiCO and SiCN based materials have lower k values than silicon nitride (SiN). In addition, they may be deposited at higher deposition rates and at lower deposition temperatures. By using the SiCO and SiCN based materials in the MOS device, the characteristics of the device such as the outer fringing capacitance, contact resistance, sheet resistance, threshold voltage, and leakage current are either improved or comparable to the prior art.

[0007] In the preferred embodiment, a gate dielectric and a gate electrode are formed on a substrate. A pair of spacers is formed along opposite sidewalls of the gate electrode and gate dielectric. The source and drain are formed. A contact etch stop (CES) layer is formed on the source/drain regions and spacers. The CES layer is preferably formed of SiCO based material or SiCN based material. An inter-level dielectric (ILD) is formed on the CES layer. The contact openings are then formed and contact plugs are formed in the contact openings.

[0008] SiCO and SiCN based materials may also be used to form other parts of the MOS device, such as spacers, gate step features and the ILD.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0010] Figures 1 through 7 are cross-sectional views of intermediate stages in the manufacture of a preferred MOS transistor embodiment;

[0011] Figures 8a and 8b illustrate models for the fringing capacitance;

[0012] Figure 9 illustrates the fringing capacitances as a function of the spacing between poly and source/drain/poly;

[0013] Figure 10 illustrates the cumulative probability as a function of the contact resistance between an n+ doped source/drain and a contact plug; and

[0014] Figure 11 illustrates the cumulative probability as a function of the contact resistance between a p+ doped source/drain and a contact plug.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0015] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0016] The preferred embodiments of the present invention use silicon oxycarbide (SiCO) and silicon carbonitride (SiCN) based material, such as carbon-doped oxide (CDO) and nitride-doped silicon carbide (NDC) to make MOS devices. The details of making the preferred embodiments are discussed. The test results of the MOS devices are then discussed.

[0017] Figures 1 through 7 illustrate the preferred embodiments of the present invention. Figure 1 illustrates the formation of a gate. In an illustrative embodiment, the substrate 2 is a silicon substrate. In other embodiments, silicon germanium (SiGe), bulk semiconductor, strained semiconductor, compound semiconductor, multi-layer semiconductor or silicon-on-insulator (SOI), strained silicon-on-insulator (SSOI), strained silicon germanium on insulator (S-SiGeOI), silicon germanium on insulator (SiGeOI), germanium on insulator (GeOI) and similar materials can be used as the substrate 2. As is known in the art, portions of the substrate, such as channel areas, will be lightly doped with n or p type dopant.

[0018] A gate dielectric 4 is deposited on the surface of substrate 2. The gate dielectric may preferably be oxide. The forming method can be any of the known methods, such as local oxidation of silicon (LOCOS), chemical vapor deposition (CVD), etc. In another embodiment, silicon nitride is used since it is an effective barrier to impurity diffusion. The silicon nitride film

is preferably formed by thermal nitridation of silicon. It can also be prepared by plasma anodic nitridation using nitrogen-hydrogen. The silicon nitride film may also be formed by thermal nitridation of SiO_2. In other embodiments, the gate dielectric may also be an oxy-nitride, an oxygen-containing dielectric, a nitrogen-containing dielectric or any combination thereof.

[0019] Figure 1 also shows a gate electrode 6 formed on gate dielectric 4. Gate electrode 6 is preferably polysilicon, although it may be formed of metal, or a compound structure comprised of metal, semiconductor, metal oxide and silicide. A preferred method of formation is chemical vapor deposition (CVD). The polysilicon has the ability of being used as a mask to achieve minimum gate-to-source/drain overlap. This in turn enhances the device performance. The polysilicon is then doped to reduce the sheet resistance. Other embodiments may use amorphous silicon, elemental metals that are conductive, alloys of elemental metals that are conductive, silicides or nitrides of elemental metals that are conductive or any combination thereof. The gate polysilicon 6 and gate dielectric 4 are patterned to form a gate.

[0020] Figure 2 illustrates a gate with spacers. A pair of spacers 8 is formed along the sidewalls of the gate dielectric 4 and gate electrode 6. Spacers 8 serve as self-aligning masks for a subsequent salicidation process, as described below. The spacer material can be oxide, silicon nitride, oxy-nitride or any combination thereof. The spacers 8 may be formed by well-known methods such as blanket depositing a dielectric layer over the entire region including substrate 2 and gate electrode 6, then anisotropically etching to remove the dielectric layer from horizontal surfaces and leaving the spacers 8.

[0021] In the preferred embodiment, the spacer material can be SiCO based, such as carbon-doped oxide (CDO), carbon incorporated silicon oxide (SiOC) or Ornithine decarboxylase (ODC). In another preferred embodiment, the spacer material can be SiCN based, such as

nitrogen-doped silicon carbide (NDC). The details of forming the SiCO and SiCN based layer are provided below with the introduction of the formation of the CES. The k value of the SiCO and SiCN based material is preferably smaller than about 5.0. Since the typical integrated circuit size is decreasing, the typical distance between the contact plugs (i.e., the conductive contacts to the source and drain, respectively) and poly is also decreasing, so that the outer fringing capacitance (the capacitance between the gate poly and the source/drain) becomes more significant. The reduction of the k value helps the reduction of the outer fringing capacitance. Therefore, lower k value materials are preferred. In the preferred embodiment, when the spacer material is changed from silicon nitride, which has a k value of 7.5, to a SiCO or SiCN based material with a k value of 4.0, the outer fringing capacitance is reduced by about 4% to about 5%.

[0022] The SiCO and SiCN based materials are not limited to the spacers. If the gate structure of the device has a dielectric step feature that is either between one poly layer and another poly layer, or between a poly and a contact plug, then it is desirable that the step feature be made of SiCO or SiCN based materials. A step feature is a feature that rises above the silicon substrate. Preferably, SiCO and SiCN based materials may be used if the spacing between the spacers of the neighboring devices is smaller than about 300Å, or the step feature has an aspect ratio (the ratio of step height to step length) larger than about 2, or the step height is larger than about 300Å. In a typical case, a step feature may have a height of greater than about 1000Å. Also when a CESL is deposited on polysilicon gates that do no have spacers formed, the CESL deposited at the sidewall of the poly becomes the step feature and SiCO and SiCN based materials are desired to be used as the CESL.

[0023] Figure 3 illustrates the formation of the source and drain. A semiconductor material 10, which defines the regions of the source and drain, is epitaxially deposited. A preferred

method of forming semiconductor material 10 is selective epitaxy. A SiO_2 layer (not shown) is formed to cover substrate 2. Openings are then formed through the SiO_2 to expose source/drain regions. Semiconductor material 10 is then epitaxially grown. Semiconductor material 10 is preferably formed using molecular beam epitaxy (MBE), although other deposition techniques, including chemical vapor deposition (CVD), ultra high vacuum chemical vapor deposition (UHVCVD), atomic layer chemical vapor deposition (ALCVD) or metal organic chemical vapor deposition (MOCVD) can also be used. In the region where a single crystal substrate is exposed, semiconductor 10 is grown epitaxially. On the SiO_2 layer, a poly-crystal is formed. The poly-crystal and SiO_2 are then etched, leaving only semiconductor layer 10. In other embodiments, source 9 and drain 11 can be formed of materials that are epitaxially grown in recesses formed in substrate 2, in which case the source 9 and drain 11 are formed substantially within substrate 2 (as opposed to on substrate 2). In yet other embodiments, source 9 and drain 11 can be formed by doping select regions of substrate 2.

[0024] Gate electrode 6 and source 9 and drain 11 regions are then exposed to ion-implantation. It is desirable that the source 9 and drain 11 regions formed from semiconductor material 10 be highly doped with p or n type dopant. The resistivity of the polysilicon is reduced through doping. An annealing step is then performed to restore lattice structure to the pre-implanted state. The annealing process is carefully controlled. In one embodiment, the dopant is diffused vertically beyond the implant-damaged region. In another embodiment, a rapid thermal process (RTP) is adopted to minimize dopant redistribution. It is to be appreciated that lateral distribution may cause dopant to diffuse into the region under the spacers, but may not be diffused to the region under the gate dielectric.

[0025] Also shown in Figure 3, silicide regions 13 are formed through a self-aligned silicide (salicide) process. The gate electrode and source and drain regions are coated with a transitional metal, such as Cobalt, Titanium, Nickel, or the like. In the preferred embodiment, Nickel is used. The device is then heated, which causes the metal to react with the underlying silicon and form a silicide. The un-reacted metal is selectively removed through the use of an etchant that does not attack the silicide, SiO_2 and silicon substrate, as is well known in the art.

[0026] Pretreatments may be optionally performed. An H_2 pretreatment may preferably be conducted in a chamber. One example of the treatment condition is: The H_2 flow rate is about 9500sccm, the chamber pressure is kept at about 2.3torr, the temperature is about 400ºC and the treatment time is about 10 seconds.

[0027] An NH_3 pretreatment may also be performed optionally under the following conditions. The chamber is filled with combined gases of NH_3 and N_2, the NH_3 flow rate is about 9500sccm, and the N_2 flow rate is about 2800sccm. The chamber pressure is kept at about 4.8torr. The temperature is about 400ºC and the treatment time is about 10 seconds.

[0028] Figure 4 illustrates the formation of a glue layer 14. To improve adhesion and prevent the CES layer from peeling, a thin glue layer 14 of SiC may optionally be formed on the whole device including source 9 and drain 11 regions, gate spacer 8 and poly 6. The glue layer 14 may be formed by plasma enhanced chemical vapor deposition (PECVD), or other methods such as atomic layer deposition (also known as atomic layer chemical vapor deposition or ALD), low pressure CVD (LPCVD). Preferably, PECVD is used. One example of the deposition conditions is: the precursor is $Si(CH_3)_4$ (also known as 4MS or tetramethysilane), the flow rate of 4MS is about 1350sccm, and the chamber pressure is kept at about 1.6torr. The temperature is

about 400ºC and the treatment time is about 20 seconds. The thickness of the glue layer 14 is preferably 20Å to about 50 Å, and more preferably about 20Å.

[0029] As shown in Figure 5, a contact etch stop (CES) layer 16 is blanket deposited on glue layer 14. CES layer 16 is preferably formed by PECVD, or other methods such as ALD or LPCVD. In one preferred embodiment of forming the CES layer 16, the material of the CES layer 16 is carbon-doped oxide such as CDO, SiOC, and ODC. CES layer 16 is preferably deposited to a thickness of about 100Å to about 1000Å, and more preferably about 300Å. The forming gas may be any carbon containing precursor, preferably gases comprising 4MS or $(CH_3)_3SiH$ (also known as 3MS or tetramethylsilane) and carbon dioxide (CO_2). In a preferred embodiment where a CDO film is deposited, the gas chamber may be filled with gas precursor of 4MS and CO_2. The flow rate of the gas precursor is about 1060sccm to about 3860sccm. The chamber pressure is maintained at about 1.5torr. The deposition temperature is about 400ºC. Under these conditions, a 300Å to 500Å CDO film takes about 10 seconds to about 50 seconds to be deposited.

[0030] In another preferred embodiment of forming the CES layer 16, the material of CES layer 16 is nitrogen-doped oxide such as NDC and SiCN. The CES layer 16 is preferably deposited to a thickness of about 100Å to about 1000Å, and more preferably about 300Å. The forming gas may be any carbon containing precursor, preferably gases comprising 4MS or $(CH_3)_3SiH$ (also known as 3MS or tetramethylsilane), NH_3 and N_2. In a preferred embodiment where an NDC film is deposited, the gas chamber may be filled with gas precursor of 4MS, NH_3 and N_2. The flow rate of the gas precursor is about 1120sccm to about 1700sccm. The chamber pressure is maintained at about 3.9torr. The deposition temperature is about 400ºC. Under these conditions, a 300Å to 500Å NDC film takes about 10 seconds to about 50 seconds to deposit.

[0031] The k value of the SiCO and SiCN based materials is lower than the k value of silicon nitride (typically 7.5 to 8), and the actual k value varies from one process to another. The k value may be adjusted by changing the forming conditions such as the deposition pressure, and the k value of the resulting film typically ranges about 3.0 to about 5.0.

[0032] The addition of the CES layer 16 causes inherent stress in the device. It is known that the stress in the device can enhance the carrier mobility, therefore enhancing the device performance. It is also known in the art that the in-plane tensile stress improves the performance of an NMOS device while it degrades the performance of a PMOS device. Therefore, it is desirable that the stress caused by the CES layer 16 be adjustable in order to make use of the beneficial effect of the stress. In the preferred embodiment, the stress may be adjusted by adjusting the deposition conditions such as the deposition temperature. The stress can be adjusted in a range of about –3Gpa to about 3Gpa, where the positive value indicates tensile stress and the negative value indicates compressive stress.

[0033] Next, as shown in Figure 6, an inter-level dielectric (ILD) layer 18, also sometimes known as a pre-metal dielectric (PMD) or an inter-metal dielectric (IMD) layer is deposited on the surface of CES layer 16. In a preferred embodiment, ILD layer 18 is a SiCO or SiCN based material with a k value smaller than about 7.0. More preferably, the k value is smaller than about 4.0. As known in the art, ILD layer 18 provides insulation between the transistor and the overlying metal lines that are formed subsequently. Parasitic capacitors exist between the source/drain and poly and metal lines formed on ILD layer 18, and the parasitic capacitance degrades the device performance. Lowering the k value of the ILD layer 18 makes the parasitic capacitance smaller, therefore improving the device performance. Since a capacitance is proportional to the k value of the dielectric material used, the reduction of the parasitic

capacitance may be significant. In other embodiments, ILD layer 18 may also be silicon dioxide deposited using, e.g., Tetraethyl Orthosilicate (TEOS), CVD, PECVD, LPCVD, or other well-known deposition techniques.

[0034] Also shown in Figure 6 is a photo resist material 20 formed and patterned on ILD layer 18 in order to form contact openings 24 to the source and drain regions and the gate. Since ILD layer 18 and CES layer 16 are different materials that can be selectively etched, the etching is performed in two steps. First, the ILD layer 18 is etched stopping at CES layer 16. Second, the CES layer 16 is etched through to expose the underlying layer. Since CES layer 16 is thin compared to ILD layer 18, etching can be controlled more precisely to prevent over etching. Although the materials of CES layer 16 and ILD layer 18 may both be SiCO and SiCN based, they must be different so that selective etching can be performed. In one embodiment, ILD layer 18 is SiCO and CES layer 16 is SiCN, so that when etching ILD layer 18 using $C_4F_6 + O_2 + CO + Ar$, the etching stops at CES layer 16. CES layer 16 can then be etched using $CH_2F_2 + O_2$.

[0035] As shown in Figure 7, contact plugs 24 are formed in the contact openings. Contact plugs 24 may be formed of tungsten, aluminum, copper, or other well-known alternatives. Contact plugs 24 may also be composite structures, including, e.g., barrier and adhesion layers, such as titanium / titanium nitride or tantalum nitride, and other layers as well.

[0036] The preferred embodiments of the present invention are compared to the prior art in several aspects such as the k value, parasitic capacitance, deposition rate, contact resistance, sheet resistance, etc. Each of the aspects is discussed briefly below. The prior art devices are formed with similar structures and under similar conditions as the preferred embodiments unless specified otherwise.

[0037] Table 1 shows the forming parameters and results of three materials, SiN, ODC and NDC, where SiN is the material used in the prior art, and ODC and NDC are materials used by the preferred embodiments of the present invention. The SiN film is formed in a gas chamber filled with precursor SiH_4, NH_3 and N_2. The deposition temperature is about 480ºC and the chamber pressure is kept at about 3torr.

TABLE 1

Material	SiN	ODC	NDC
Deposition time (Second)	176	54	31
Thickness (Å)	1207	1171	1104
Deposition rate (Å/Minute)	411	1301	2137
k Value	7.5 ~ 8	4 ~ 5	4 ~ 5
Deposition temperature (ºC)	480	400	400

[0038] It is noticed that in the preferred embodiments of the present invention, the deposition of the CES layer 16 is faster and may be performed at lower temperatures. The deposition rate of ODC and NDC is about 4 to 5 times the deposition rate of SiN and the deposition temperature of ODC and NDC is 400ºC, which is lower than the 480ºC for SiN. The k value of ODC and NDC is in the range of about 4 to 5, much lower than the k value of SiN, which is in the range of about 7.5 to 8.

[0039] The outer fringing capacitance (parasitic capacitance between poly 6 and source/drain 10) of the device is reduced in the preferred embodiment of the present invention.

Figures 8a and 8b illustrate the models used to explain the fringing capacitance results. Each of the figures contains spacers of two neighboring MOS devices. In Figure 8a, 48 and 50 are spacers, and a contact plug 60 is connected to a source or drain 54. Distance d_1 is the distance between poly 42 and contact plug 60. Between poly 42 and contact plug 60, there exists fringing capacitance 30. Figure 8b is similar to Figure 8a except contact plug 60 is removed. Distance d_2 is the distance between poly 62 of one device and poly 73 of another device. Between poly 62 and poly 73, there exists fringing capacitance 80. There are also outer fringing capacitances (the parasitic capacitance between poly and source/drain) 32 between poly and source/drain.

[0040] The capacitances measured are illustrated in Figure 9, which shows the fringing capacitance as a function of the spacing between source/drain/poly and poly. (The spacing is d_1 in Figure 8a and d_2 in Figure 8b.) Line 1 and line 2 are the fringing capacitances shown in Figure 8a, and the fringing capacitance is the combination of capacitances 30 and 32. The k value of CES layer 46, which is formed of SiN, is 7.5 for line 1, and the k value of CES layer 46, which is formed of CDO or NDC, is 4.0 for line 2. Line 3 and line 4 are the fringing capacitances shown in Figure 8b, and the fringing capacitance is the combination of capacitances 80 and 32. The k value of CES layer 46, which is formed of SiN, is 7.5 for line 3, and the k value of CES layer 46, which is formed of CDO or NDC, is 4.0 for line 4. It is observed that CES layer 46 contributes to the capacitance 30, so that lowering the k value of CES layer 46 reduces the capacitance 30. Therefore, line 2 is lower than line 1 since the k value of CES layer 46 for line 2 is lower. The difference between the capacitances in lines 1 and 2 is about 4% to about 5%. Also, line 4 is lower than line 3 because the k value of CES layer 66 for line 4 is lower than the k value of CES layer 66 for line 3. When the spacing increases, the capacitance of 30 and 80 decreases so that the effect of the CES layer is reduced. At some point, the spacing increases significantly enough

that the effects of capacitance 30 and 80 diminish and capacitance 32 becomes the major portion of the fringing capacitance. Therefore, lines 1, 2, 3 and 4 merge.

[0041] It is known in the art that CES layer 16 affects the contact resistance between its underlying layers 6, 10 and the contact plugs 24, possibly because it affects the contact surface characteristics, the contact shape and the over-etch behavior. The contact resistance between the contact plugs 24 and the source/drain 9, 11 are also compared to the prior art. The result is shown in Figures 10 and 11. Figure 10 illustrates the cumulative probability as a function of the contact resistance between a contact plug 24 and an n+ doped source/drain 10. The result is based on 794,475 serially connected contacts. It is noted that the contact resistance with ODC (shown as line 81) or NDC (shown as line 82) as the CES layer 16 is about 10% lower than the contact resistance with SiN (shown as line 83) as the CES layer 16.

[0042] Figure 11 illustrates the cumulative probability as a function of contact resistance between a contact plug 24 and a p+ doped source/drain 9, 11. The result is also based on 794,475 serially connected contacts. The contact resistance with NDC (shown as line 91) and ODC (shown as line 92) as the CES layer 16 is noticeably smaller than the contact resistance of SiN (shown as line 93) as the CES layer 16.

[0043] Contact resistance also exists between n+ doped poly silicon and the metal contact. From the test performed based on the average of 794,475 contacts connected in series, it is found that the resistance of NDC and ODC is a little better than the contact resistance of SiN, so that the contact resistance between metal and p+ and n+ poly silicon is at least comparable to the prior art.

[0044] The test also shows that when the material of the CES layer 16 is changed from SiN to ODC or NDC, the sheet resistances of the underlying materials are not affected. Measurements

have been conducted on n+ source/drain, p+ source/drain, n+ doped poly silicon and p+ doped poly silicon. Their sheet resistances do not change regardless of the materials of the overlaying CES layer.

[0045] Other characteristics, such as the threshold voltage and the leakage current of the resulting MOS transistor were also tested. No substantial difference was found between different CES layer materials, such as ODC, NDC and SiN.

[0046] Besides the advantages mentioned above, the preferred embodiments of the present invention are fully compatible with current device fabrication processes, and can be made by existing tools and known methods, so that there is no extra cost involved.

[0047] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:

a substrate having a surface;

a gate dielectric formed on the surface of the substrate;

a gate electrode formed on the gate dielectric;

a pair of spacers formed along opposite sidewalls of the gate electrode and the gate dielectric;

source and drain regions formed on opposite sides of the gate electrode;

a contact etch stop (CES) layer blanket formed on the source and drain regions and the spacers wherein the CES layer is formed of a material selected from the group consisting essentially of a silicon oxycarbide (SiCO) based material and a silicon carbonitride (SiCN) based material;

an inter-level dielectric (ILD) formed on the CES layer; and

a conductive plug formed in the inter-level dielectric.

2. The integrated circuit device of claim 1 wherein the spacer material is a material selected from the group consisting essentially of a Silicon, Carbon containing based oxide and a Silicon, Carbon containing based nitride and having a dielectric constant (k value) smaller than about 5.0.

3. The integrated circuit device of claim 1 further comprising a glue layer formed on the CES layer.

4. The integrated circuit device of claim 3 wherein the glue layer material is SiC.

5. The integrated circuit device of claim 3 wherein the glue layer has a thickness of about 20Å to about 50Å.

6. The integrated circuit device of claim 1 wherein the CES layer has a k value less than about 7.0.

7. The integrated circuit device of claim 1 wherein the thickness of the CES layer is between about 100Å to about 1000Å.

8. The integrated circuit device of claim 1 wherein the CES layer has an inherent stress between about –3GPa and 3GPa.

9. The integrated circuit device of claim 1 further comprising a step feature comprising a material selected from the group consisting essentially of a Silicon, Carbon containing based oxide and a Silicon, Carbon containing based nitride and having a k value less than about 5.0.

10. The integrated circuit device of claim 9 wherein the step feature has a height greater than about 300Å.

11. The integrated circuit device of claim 9 wherein the step feature has an aspect ratio greater than about 2.

12. The integrated circuit device of claim 9 further comprising:

a second gate electrode formed over a second gate dielectric and having a second pair of spacers formed along opposite sidewalls of the gate electrode and the gate dielectric, wherein one

of the spacers of the second pair of spacers is spaced apart from one of said pair of spacers by at most 300Å.

13. The integrated circuit device of claim 1 wherein the ILD material comprises a material selected from the group consisting essentially of a Silicon, Carbon containing based oxide and a Silicon, Carbon containing based nitride.

14. A method of forming an integrated circuit device comprising:

forming a gate dielectric on a surface of a substrate;

forming a gate electrode on the gate dielectric;

forming a spacer along a sidewall of the gate electrode and the gate dielectric;

forming a source/drain region adjacent the spacer;

forming a contact etch stop (CES) layer over the source/drain region and the spacer wherein the CES layer comprises a material selected from the group consisting essentially of a silicon oxycarbide (SiCO) based material and a silicon carbonitride (SiCN) based material;

forming an inter-level dielectric (ILD) on the CES layer; and

forming a conductor in the inter-level dielectric.

15. The method of claim 14 wherein the CES layer is formed by chemical vapor deposition (CVD).

16. The method of claim 15 wherein the CVD method is selected from the group consisting of plasma enhanced CVD (PECVD), atomic layer deposition (ALD), and low pressure CVD (LPCVD).

17. The method of claim 16 wherein the CES layer is deposited in a precursor comprising carbon containing materials.

18. The method of claim 17 wherein the precursor comprises Si(CH3)4 (4MS) and SiH(CH3)3 (3MS).

19. The method of claim 16 wherein the deposition temperature is between about 300ºC to about 800ºC.

20. The method of claim 14 further comprising a H_2 plasma pretreatment prior to the step of forming the CES layer.

21. The method of claim 14 further comprising a NH_3 plasma pretreatment prior to the step of forming the CES layer.

22. The method of claim 14 further comprising forming a SiC glue layer prior to the step of forming the CES layer.

23. The method of claim 14 wherein the CES layer has an inherent stress between about -3GPa to about 3GPa.

24. The method of claim 14 wherein the spacer material is a material selected from the group consisting essentially of a SiCO based material and a SiCN based material and wherein the spacer material has a k value less than about 5.0.

25. The method of claim 14 further comprising a step of forming step features wherein the step feature material is SiCO or SiCN based material having a k value smaller than about 5.0.

26. The method of claim 14 further comprising:

forming at least two transistor devices having spacers wherein the spacing between the spacer of the first transistor device and the spacer of the second transistor device is smaller than about 300Å.