METHOD FOR FABRICATING SEMICONDUCTOR DEVICES

WITH REDUCED JUNCTION DIFFUSION

ABSTRACT

A transistor which includes halo regions disposed in a substrate adjacent to opposing sides of the gate. The halo regions have upper and lower regions. The upper region is a crystalline region with excess vacancies and the lower region is an amorphous region. Source/drain diffusion regions are disposed in the halo regions. The source/drain diffusion regions overlap the upper and lower halo regions. This architecture offers the minimal extension resistance as well as minimum lateral diffusion for better CMOS device scaling.

Figure 5