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ABSTRACT OF THE DISCLOSURE



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A digital reproduction signal processor relating to the present invention is provided with an analog/digital converter 4 for sampling an analog reproduction signal at a period which is longer than a digital recording channel rate, to convert to a low rate digital reproduction signal having a period which is longer than a recording channel rate, a coefficient setting unit 6 for performing a digital filtering with keeping the low rate, to generate a digital equalization signal, and an interpolator 7 for interpolating a reproduction data of the digital recording channel rate, and a half-rate Viterbi decoder 8 for taking out data.

According to the digital reproduction signal processor constructed as above, even when a digital read channel employing a PRML is employed, the analog/digital converter 4 or a digital circuit operated at a channel rate can be eliminated, thereby to provide a reproduction signal processor operating with low power consumption and of low cost.