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[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR ON-CHIP PHASE ERROR MEASUREMENT TO DETERMINE JITTER IN PHASE-LOCKED LOOPS

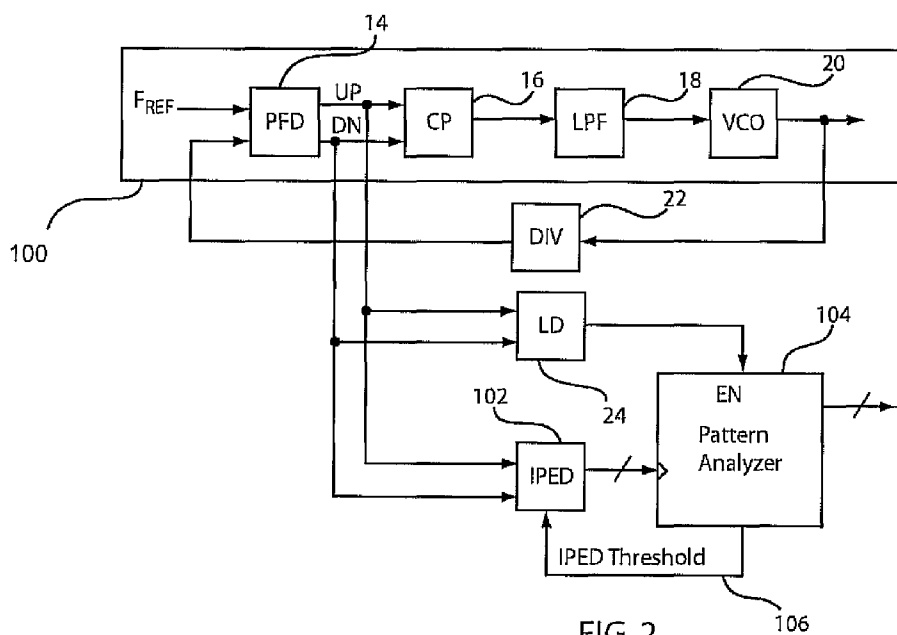


FIG. 2

(57) Abstract: An apparatus includes a phase-locked loop, PLL, circuit (100) including a phase-frequency detector configured to output phase error signals. A phase error monitor circuit (102) is configured to determine instantaneous peak phase error by logically combining the phase error signals and comparing pulse widths of the logically combined phase error signals to a programmable delay time at each reference clock cycle to determine instantaneous phase error change. A storage element (124) is configured to store the instantaneous phase error change.

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