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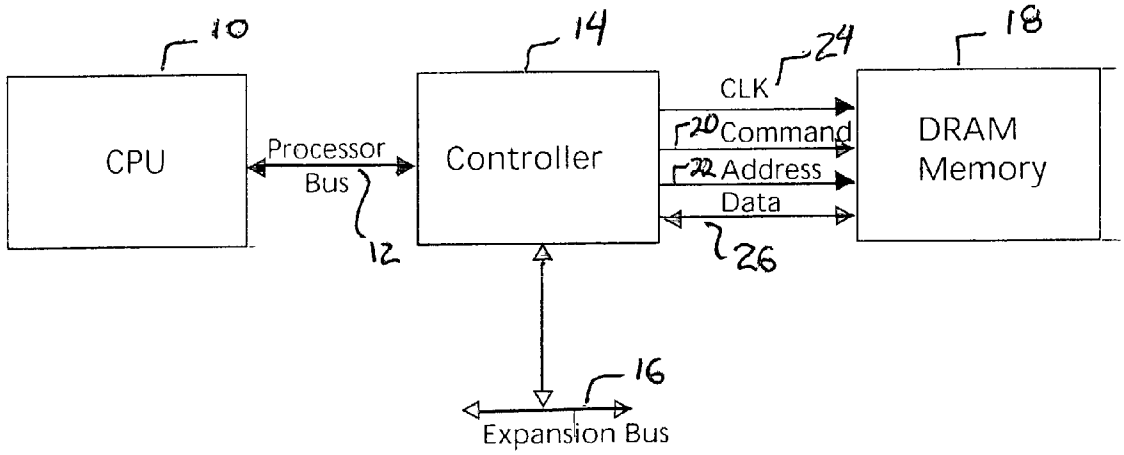
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(54) Title: SEQUENTIAL NIBBLE BURST ORDERING FOR DATA



(57) Abstract: A memory device is comprised of a plurality of arrays of memory cells and peripheral devices for reading information out of and for writing information into the memory cells. The peripheral devices include a decode circuit responsive to a first portion of address information for identifying an address and is further responsive to a second portion of the address information for identifying an order. The address may by a read address or a write address, and the order may be the order for reading data or writing data, respectively. The peripheral devices may also include a read sequencer circuit or both a write sequencer circuit and a read sequencer circuit for reordering bits to be read or written, as the case may be, in response to another portion of the address information. The necessary address information is routed to the sequencer circuits by an address sequencer. Methods of operating such a memory device are also disclosed.

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