

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
16 March 2023 (16.03.2023)



(10) International Publication Number
WO 2023/037240 A1

- (51) **International Patent Classification:**
H01L 23/34 (2006.01) *H01L 21/50* (2006.01)
- (21) **International Application Number:**
PCT/IB2022/058368
- (22) **International Filing Date:**
06 September 2022 (06.09.2022)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
202141040790 08 September 2021 (08.09.2021) IN
- (72) **Inventor; and**
- (71) **Applicant: BOLLOJU, Vijay** [US/IN]; Flat No.1123, Sobha Petunia, Veeranapalya, Nagavara Village, BEL HQ, Arabic College, Bengaluru 560045 (IN).
- (74) **Agent: RAJU, Chandrasekhar;** Chandrasekhar Raju, Pat-nTech, #326,4th B, Cross, 3rd Block, HRBR, Layout, Kalyan Nagar, Bengaluru 560043 (IN).
- (81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.
- (84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH,

(54) **Title:** SUBSTRATELESS HYBRID POWER MODULE ASSEMBLY AND METHOD FOR FABRICATING THEREOF

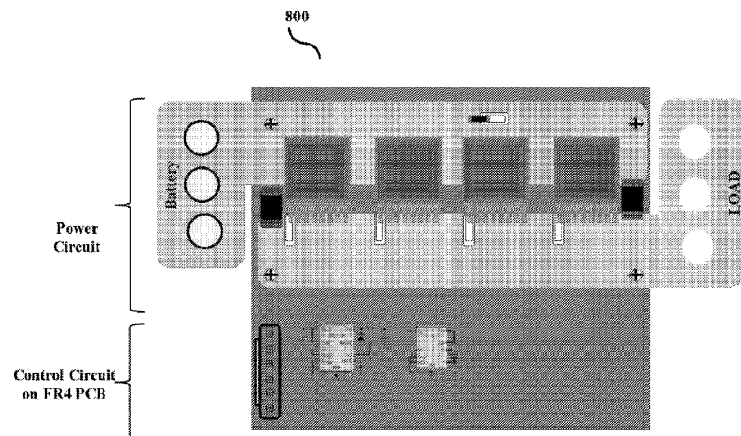


FIG. 8

(57) **Abstract:** Embodiments herein disclose a method for fabricating a substrateless hybrid power module assembly. The method includes providing a PCB (1302). Further, the method includes assembling a control circuit component on the PCB (1302). Further, the method includes attaching a power device on the control circuit component. Further, the method includes performing device interconnects on the device using SMT a wire bonding and/or a copper strap. Further, the method includes attaching a busbar on a bottom portion of the PCB (1302). Further, the method includes attaching an isolation layer (1312) below the busbar attached on the bottom portion of the PCB (1302). Further, the method includes attaching a heat dissipating layer (1314) below the isolation layer (1312). Further, the method includes attaching one of a plastic moulding case (2702) and a potting compound on the heat dissipating layer (1314).

[Continued on next page]

GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to the identity of the inventor (Rule 4.17(i))*
- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*
- *of inventorship (Rule 4.17(iv))*

Published:

- *with international search report (Art. 21(3))*
- *in black and white; the international application as filed contained color or greyscale and is available for download from PATENTSCOPE*