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(72) Inventor; and

(71) Applicant: RAMIREZ, Juan Pablo [US/MX]; Agustin
Lara #5780, Col. La Estancia, Zapopan, Jalisco, 45030
(MX).

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(54) Title: SIMPLE AND LINEAR FAST ADDER

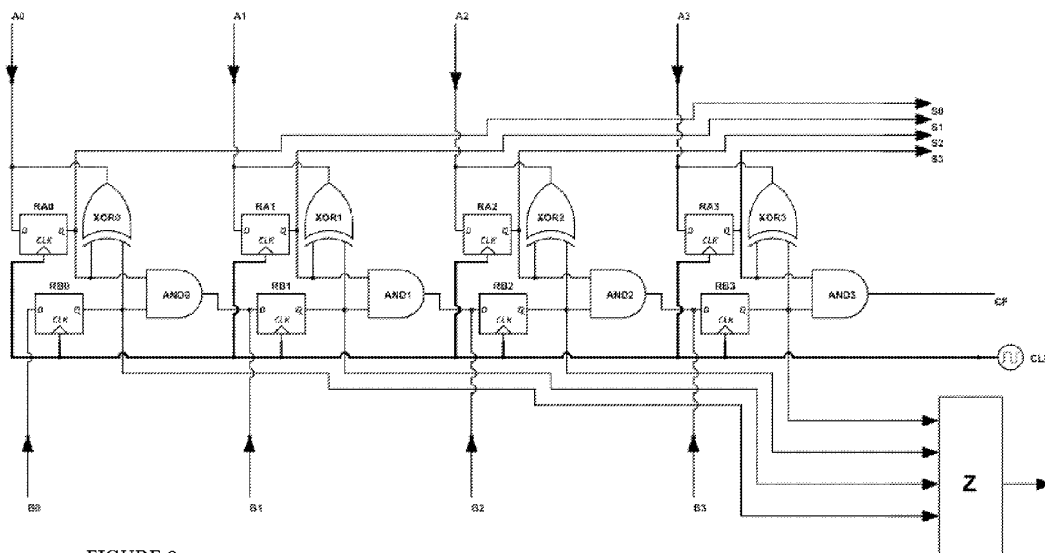


FIGURE 9

(57) Abstract: Disclosed herein is a fast adder design based on a novel axiomatization of mathematics, of natural and real numbers, by the author. Addition is a Finite State Machine that, on an average, takes $\log_2 n$ iterations to calculate a n -bit addition. Further, for the proposed fast adder, the probability of a n -bit addition taking $k \leq n$ iterations to complete, is equal to the probability of k consecutive heads in n fair coin tosses. The circuitry is linear and simple, in the sense that adding bits to the inputs does not complicate the circuit topology. The growth is linear, and the instruction set is constant, and hardware based.

[Continued on next page]

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