ABSTRACT

INTERPOLATION METHOD AND CIRCUIT

An interpolation circuit for an optical encoder or other sensing device includes a signal generating circuit (140), a comparator circuit (142) and a logic circuit (15). The signal generating circuit (140) generates A, A′, B, B′, one or more fractional A or A′ and one or more fractional B or B′ ramp signals in response to input ramp signals that are one quarter cycle out of phase. The comparator circuit (142) compares selected pairs of the A, A′, B, B′, one or more fractional A or A′ and one or more fractional B or B′ ramp signals and generates intermediate signals. The phases of the intermediate signals are preferably uniformly or nearly uniformly distributed in phase with respect to the ramp signals. The logic circuit (15) combines the intermediate signals and provides first and second output signals, each having multiple cycles of the ramp signals. In one embodiment, the signal generating circuit (142) generates A, A′, B, B′, A/3 or A′/3 and B/3 or B′/3 ramp signals. The logic circuit (15) provides first and second output signals having a total of 16 states, thereby providing a resolution of 16 states for each cycle of the ramp signals.

Figure 4