

CONTROL CIRCUIT AND METHOD

Abstract of the Disclosure

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(with reference to the drawing of FIG.1)

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A control circuit (10) for use with a digital telecommunications device comprises a number of memory addresses (20) coupled to receive data from a source (30) and an addressing circuit (40) for addressing the memory addresses (20). A time divided transmitter (45) is arranged to read the data from the memory addresses (20) and to transmit the data at a selected one of a number of periodic time divided slots. A control circuit (80) controls the transmitter (45) and the addressing circuit (40). The control circuit (80) selects one of the slots and causes the addressing circuit (40) to offset the addressing of the plurality of memory addresses (20).

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