

PATENT SPECIFICATION

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- (21) Application No. 26688/75 (22) Filed 24 June 1975
(31) Convention Application No. 2 435 279 (32) Filed 23 July 1974 in
(33) Fed. Rep. of Germany (DE)
(44) Complete Specification published 4 May 1978
(51) INT. CL.² H03K 21/14
(52) Index at acceptance
G4D 6C1 6C2 6Y



(54) IMPROVEMENTS IN OR RELATING TO DIGITAL COUNTING ARRANGEMENTS

(71) We, LICENTIA PATENT-
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BESCHRANKTER HAFTUNG, a company or-
ganised under the laws of Germany, of
Theodor-Stern-Kai 1, 6 Frankfurt/Main 70,
Germany, do hereby declare the invention,
for which we pray that a patent may be
granted to us, and the method by which it
is to be performed, to be particularly de-
scribed in and by the following
statement:—

The present invention relates to digital
counting arrangements using electronic
digital counters to count pulses and is es-
pecially, though not exclusively applicable
to the use of such counters in association
with digital display devices for the digital
display of frequency in telecommunications
receivers.

It is known, to count pulses by means of
electronic counters, also called digital coun-
ters. In this way a digital display is pos-
sible of, e.g. frequency in telecommunica-
tions apparatus (Radio Mentor 1973, pages
389-390 and Funk-Technik 1971, pages
157-159), by converting received oscil-
lations into pulses — viz. digital signals —
and counting them. In such circuits there
are normally provided divider stages which
subdivide the number of pulses before they
are fed to the actual counter stages. A
counter stage may have, for example, four
output terminals at which the counter state
is indicated in the form of digital signals,
which are indicated by '1' or '0' in the
BCD code. At the end of each counting
operation the counter state, by means of
shift pulses can be transferred serially
as a pulse sequence to a store, decoded
and displayed optically on a display de-
vice. This may be achieved by a multiplex
procedure.

It is an object of the invention to
provide a simpler form of the electronic

counter circuits of the type set forth above.

According to the present invention there
is provided an electronic counter, arranged
to count pulses during a predetermined
gating period, including a display device
arranged to display a plurality of digits,
each of which represents one place of the
count at the end of said gating period, and
a plurality of counter stages, each of which
is arranged to count a respective place of
the said count wherein the display device
is arranged to receive for each digit in-
formation, indicative of the state of the re-
spective counter stage, and, for the digit re-
presenting the least significant place of the
count, the display device is arranged to re-
ceive less information than is required to
display that place to the accuracy re-
presented by the state of the respective
counter stage.

In order that the invention may be
clearly understood and readily carried into
effect examples thereof will now be de-
scribed with reference to the accompanying
drawings of which,

Fig. 1 shows a simplified circuit diagram
of a counter in accordance with the in-
vention.

Fig. 2 shows a divider stage and its
digital signals at the output terminals.

The invention is based on appreciation
of the fact that in many applications it
is sufficient if the lowest value last place —
e.g. the units place — does not assume all
the possible numerical values from '0' to
'9' but for example is only a '0' or a '5'.
This applies particularly when the source
of the counting pulses is not exactly con-
stant. The last place would then fluctuate
and jump to different values, so that an
uninformed user is confused. In radio ap-
paratus with digital display of frequency it
is particularly advantageous for the fre-
quency spacings in the display to agree with
the smallest spacing of the sender

frequencies (channels). In this way the number of possible combinations of numbers is reduced to the value absolutely necessary corresponding to the maximum possible number of channels in the band in question.

In Fig. 1 a counter according to the invention is shown in an arrangement for the digital display of frequency in a radio apparatus. Oscillations received by an antenna 1 pass to an HF and IF circuit 2 and are demodulated in a demodulating circuit 3. After amplification the demodulated low frequency is reproduced through a loudspeaker 4.

The HF and IF circuit 2 includes, inter alia, an oscillator for the formation in known manner of the intermediate frequency. Pulses 6 at the oscillator frequency are taken from this oscillator, amplified and fed via a lead 5 to a gate 7. A control unit 19 controlled by a time base 25 (in this example a quartz oscillator supplies pulses via a lead 24 to the gate 7, which is thereby periodically opened (gating period) and closed. Transfer of the result of the count to a store 17 takes place when the gate 7 is closed. By programming, for example as shown in the periodical 'Radio-Mentor' 1973, pages 389-390 (subtraction or addition of the IF), it can be arranged that the received frequency of interest is displayed instead of the oscillator frequency.

The pulses 6 that pass the gate 7 during the gating period are first subdivided by means of a plurality of divider stages, two of which, 8 and 9, are shown in the Figure, and then pass to counting and shift stages 13, 14, 15, 16. Such stages, which by selective switching function either as shift registers or as so called Johnson counters, are described in more detail in German Offenlegungsschrift DT OS 2406924. They include a shift register that through its outer circuit operates in known manner as a counter (Ditrich Becker and Heinz Mäder, 'Hochintegrierte MOS-Schaltungen', Verlag Berliner Union GmbH Stuttgart, pages 132-134), for example a Johnson counter. By means of additional circuits a counter mode or a shift register mode is selectively obtained as described in the said Offenlegungsschrift. With each place (decade) of the frequency being counted there is associated a counter and shift stage 13, 14, 15, 16 which hereinafter are referred to only as counter stages when they are operating as counters. The counter state of each counter stage 13, 14, 15, 16 is for example given at its output terminals in the 8-4-2-1 BCD code, i.e. each number between zero and nine is represented by four digital signals which represent either the logical condition '0' or '1', as shown in Fig.

2b. Counter stages having other codes can be used, e.g. the so-called Johnson code by which a digit can be represented by five digital signals. After a counting operation the counter stages 13, 14, 15, 16 are switched over to their shift mode, and the digital signals representing the actual counter state of each counter stage 13, 14, 15, 16 are, by means of shift pulses, transferred to the store 17, beginning with the counter stage for the highest value place.

The evaluation of the result of the count transferred to the store is effected by a multiplex procedure. The stored pulse sequence is decoded, by a decoder included in store 17, and the individual digits are displayed sequentially on the display device 18. The shift pulses are taken from the control unit 19 and are fed to each counter stage 13, 14, 15, 16 which now acts as a shift register, and to the store and decoder 17. In the evaluation of for example a four-place counter read-out in the Johnson code from the four counter stages 13, 14, 15, 16 twenty shift pulses are necessary (five shift pulses per digit in the Johnson code) in order to transfer the counter state to the store 17 in the form of a digital pulse sequence.

Prior to the beginning of the next gating period the counter and shift stages 13 to 16 must be cancelled (reset) or brought to an output condition corresponding to the intermediate frequency. The counter stages 13 to 16 are provided with setting inputs which are controlled by the control unit 19 by means of suitable resetting pulses. The control unit 19 is controlled, for the production of its various functions — gating period, shift pulses, resetting pulses — by a time base 25, which for example includes a quartz oscillator and supplies periodic timing pulses to the control unit 19.

In accordance with the invention, in Fig. 1 there are taken from the counter stage for the lowest value last place, of the result of the count to be displayed on the display on the display device 18, fewer pieces of information than are necessary for the exact display of the counter state of this counter stage. It will be assumed that the result of counting has five places. The four higher value digits are counted by the four counting stages 13 to 16. For the counter stage for the lowest value digit (e.g. the units place) there is provided the last decadic divider stage 9 which is arranged directly before the counter stages 13 to 16. Such a decadic divider stage is shown for example in Fig. 2a, Fig. 2b shows the logical signals at its outputs A, B, C, D in accordance with the pulses fed to it. In the example of Fig. 1 the output C is connected to the counting input of the counter stage 13.

(13)

The result of counting may for example be '74362', i.e. the counter stages 13, 14, 15, 16 have the counter states '6', '3', '4', '7' respectively, whilst the counter state of the divider stage 9 is the digit '2'. This digit '2' which represents the lowest value place corresponds to the pieces of information (logical signals) 0010 at the outputs D, C, B, A. Since only the output C is connected to the following counter stage 13 there is a logical '0' at its counter input. As above-described, the logical signals at the outputs of the counter stages 13 to 16 are transferred sequentially to the store 17 as a pulse sequence, by means of shift pulses. In the present example it is assumed that the so-called Johnson code is the basis of the counter stages 13 to 16, each digit being displayable digitally by five logical signals, so that after twenty shift pulses the contents of the four counter stages 13 to 16 are transferred to the store 17. Thereupon, by means of the following shift pulse the logical signal present at the counter input of the counter stage 13, viz. '0', is taken five times into the store. The digit '2' is therefore represented by the pulse sequence 00000. Such a pulse sequence is, in accordance with the Johnson code, recognised by the decoder 17 as the zero digit, so that the displayed result reads not '74362' but '74360'.

If the counter state of the divider stage 9 is for example '7', a logical '1' occurs at the output C. The pulse sequence taken into the store 17 would then read 11111, which is recognised by the decoder 17 as the digit '5'. In Fig. 1 therefore the digit for the last place of the result of counting will therefore be a '0' or a '5', corresponding to the possible logical state of the output C, only one piece of information being taken from the counter stage 9 associated with this place. The last divider stage 9 may thus advantageously be used as a counter stage.

The invention is of particular advantage when the components in Fig. 1 located to the right of and adjacent the chain dotted line 10 is made as an integrated module (IC) e.g. by MOS technique, and the divider stages located to the left are made as an integrated module in TTL technique. Since when using the invention only one connecting lead is necessary from the divider stage 9 to the counter stage 13, the pin number (number of terminals of the MOS-IC) can be kept small, which makes its manufacture cheaper. This is because only the one terminal 12 is necessary for transferring the counting pulses and the result of counting of the stage 9. It is not necessary to make separate provision for shift pulses for the divider stage 9, or for this stage to be capable of effecting shift-

ing. On the other hand the said subdivision into TTL-IC on the one hand and MOS-IC on the other hand may be necessary if, for example, the frequency of the pulses is too high for MOS circuits and satisfactory subdivision to a lower frequency is possible only with divider stages in TTL technique.

The solution so far described is also possible when instead of the Johnson code there is used e.g. a normal 8-4-2-1 code, the end state '1' of the output C of stage 9 being interrupted, prior to transfer to the store 17, in a sequence corresponding to the shift pulses so that the pulses sequence 101 which corresponds to the digit '5', results instead of 111. This may be effected, for example, by including in the connecting lead from the output C to the counter stage 13 a gating circuit not shown in Figure 1 which is so controlled by the shift pulses -via a monostable flip-flop circuit that the connecting lead is alternately interrupted and established at each shift pulse. With a '1' at the output C there therefore results the pulse sequence 101, which without the step described would read 111. With a '0' at the output C this step has no effect, so that the pulse sequence 000 results corresponding to the digit '0'.

It has already been mentioned that prior to the beginning of each new counting operation the counter stage 13 to 16 must be reset—this being effected by reset pulses for example taken from the control unit 19—in order that the fresh counting may begin at a definite counter state. Resetting is also necessary for the divider stages 8 to 9 that follow the gate 7. In Fig. 1 it is also possible to arrange before the gate 7 divider stages for which no resetting is then necessary. However, at least the divider stage 9 serving at the same time as counter stage for the last place must follow the gate 7.

In accordance with an advantageous development of the invention the resetting pulse for the divider stages 8, 9 is obtained from the pulse that determines the gating period. This has the advantage that in Fig. 1 no additional connection is necessary for the MOS-IC that includes the control unit 19. An additional connection would be necessary if the resetting pulse for the divider stages 8 to 9 were taken directly from the control unit 19. Since, however, the resetting pulse for the divider stages 8 to 9 is derived from the gating period, no further connection is necessary for this purpose additionally to the connection 23 which is required in any case.

In the example Fig. 1 the gate 7 is opened when a logical '1' is applied to it via a lead 24. With a logical '0' the gate 7 is closed. At the beginning of a new gating

period the potential of the lead 24 changes from '0' to '1'. This positive potential jump passes via an inverter 20, connected to the lead 24, to an RC coupling 21, 22 and thereby causes a momentary negative pulse which is fed to the divider stages 8 to 9 and reset them. Resetting of the divider stages 8 to 9 following the gate 7 therefore takes place simultaneously with the beginning of the gating period, viz. the computing period. The RC coupling 21, 22 shown is of such design that only a very short resetting pulse occurs and the condenser 21 has discharged via the resistor 22 up to the beginning of the following gating period. It is also possible to use a gate 7 that is opened for the logical state '0'. In this case the inverter 20 is omitted.

20 WHAT WE CLAIM IS:—

1. An electronic counter, arranged to count pulses during a predetermined gating period, including a display device arranged to display a plurality of digits, each of which represents one place of the count at the end of said gating period, and a plurality of counter stages, each of which is arranged to count a respective place of the said count wherein the display device is arranged to receive for each digit information, indicative of the state of the respective counter stage, and, for the digit representing the least significant place of the count, the display device is arranged to receive less information than is required to display that place to the accuracy represented by the state of the respective counter stage.

2. A counter according to Claim 1 arranged so that the said display device receives, for the least significant place of the count only sufficient information to display that place as either the digit '0' or the digit '5'.

3. A counter according to either of the preceding claims arranged to count said pulses to n places including a plurality of divider stages arranged to subdivide the said pulses, wherein the counter stages include $(n - 1)$ decadic counter stages to provide information representing the $(n - 1)$ highest places of said count and wherein one of said divider stages located directly before the $(n - 1)$ counter stages and supplying counting pulses for those stages, is effectively a counter stage arranged to provide information relating to the least significant place of said count.

4. A counter according to claim 3 wherein the $(n - 1)$ counter stages are provided as integrated MOS circuits and

the divider stages are provided as TTL circuits.

5. A counter according to either of claims 3 or 4 wherein the said one of said divider stages is a decadic counter stage having an output connected to the first of said $(n - 1)$ counter stages so that pulses applied to that divider stage are transmitted to the said first counter stage subdivided in the ratio 10:1.

6. A counter according to claim 5 including a store and wherein the said counter stages are arranged to provide the information indicative of their respective counting states to the said store, in the form of logical states '0' or '1' of the so-called Johnson code, beginning with the information indicative of the highest significant place of the said count, in response to shift pulses.

7. A counter according to claim 6 wherein, at the said display device, the digit '0' is displayed when the logical state '0' is at the output of said at least one of said divider stages and the digit '5' is displayed when the logical state '1' is at said output.

8. A counter according to claim 5 including a store means for providing shift pulses to cause the result of said count to be transferred to said store in the form of the so-called BCD code and means for interrupting the output of said one of said divider stages at alternate shift pulses so that if a logical '1' is present at said output the pulse sequence 0101, corresponding to the digit '5', is transferred to said store and with a logical '0' at said output the pulse sequence 0000, corresponding to the digit '0', is transferred to said store.

9. A counter according to any of claims 3 to 8 including an R.C. coupling comprising a capacitor in series with a resistor at a reference potential wherein the junction of the capacitor and the resistor is connected to resetting inputs of the said divider stages and pulses determining the said gating period are applied to the other terminal of the said resistor, the arrangement of the R.C. coupling being such that the capacitor is discharged other than at the change of potential at the beginning of each gating period.

10. A counter according to claim 9 wherein the said pulses determining the said gating period are applied to the said resistor via an inverter.

11. An electronic counter substantially as herein described with reference to the



period the potential of the lead 24 changes from '0' to '1'. This positive potential jump passes via an inverter 20, connected to the lead 24, to an RC coupling 21, 22 and thereby causes a momentary negative pulse which is fed to the divider stages 8 to 9 and reset them. Resetting of the divider stages 8 to 9 following the gate 7 therefore takes place simultaneously with the beginning of the gating period, viz. the computing period. The RC coupling 21, 22 shown is of such design that only a very short resetting pulse occurs and the condenser 21 has discharged via the resistor 22 up to the beginning of the following gating period. It is also possible to use a gate 7 that is opened for the logical state '0'. In this case the inverter 20 is omitted.

20 WHAT WE CLAIM IS:—

1. An electronic counter, arranged to count pulses during a predetermined gating period, including a display device arranged to display a plurality of digits, each of which represents one place of the count at the end of said gating period, and a plurality of counter stages, each of which is arranged to count a respective place of the said count wherein the display device is arranged to receive for each digit information, indicative of the state of the respective counter stage, and, for the digit representing the least significant place of the count, the display device is arranged to receive less information than is required to display that place to the accuracy represented by the state of the respective counter stage.

2. A counter according to Claim 1 arranged so that the said display device receives, for the least significant place of the count only sufficient information to display that place as either the digit '0' or the digit '5'.

3. A counter according to either of the preceding claims arranged to count said pulses to n places including a plurality of divider stages arranged to subdivide the said pulses, wherein the counter stages include $(n - 1)$ decadic counter stages to provide information representing the $(n - 1)$ highest places of said count and wherein one of said divider stages located directly before the $(n - 1)$ counter stages and supplying counting pulses for those stages, is effectively a counter stage arranged to provide information relating to the least significant place of said count.

4. A counter according to claim 3 wherein the $(n - 1)$ counter stages are provided as integrated MOS circuits and

the divider stages are provided as TTL circuits.

5. A counter according to either of claims 3 or 4 wherein the said one of said divider stages is a decadic counter stage having an output connected to the first of said $(n - 1)$ counter stages so that pulses applied to that divider stage are transmitted to the said first counter stage subdivided in the ratio 10:1.

6. A counter according to claim 5 including a store and wherein the said counter stages are arranged to provide the information indicative of their respective counting states to the said store, in the form of logical states '0' or '1' of the so-called Johnson code, beginning with the information indicative of the highest significant place of the said count, in response to shift pulses.

7. A counter according to claim 6 wherein, at the said display device, the digit '0' is displayed when the logical state '0' is at the output of said at least one of said divider stages and the digit '5' is displayed when the logical state '1' is at said output.

8. A counter according to claim 5 including a store means for providing shift pulses to cause the result of said count to be transferred to said store in the form of the so-called BCD code and means for interrupting the output of said one of said divider stages at alternate shift pulses so that if a logical '1' is present at said output the pulse sequence 0101, corresponding to the digit '5', is transferred to said store and with a logical '0' at said output the pulse sequence 0000, corresponding to the digit '0', is transferred to said store.

9. A counter according to any of claims 3 to 8 including an R.C. coupling comprising a capacitor in series with a resistor at a reference potential wherein the junction of the capacitor and the resistor is connected to resetting inputs of the said divider stages and pulses determining the said gating period are applied to the other terminal of the said resistor, the arrangement of the R.C. coupling being such that the capacitor is discharged other than at the change of potential at the beginning of each gating period.

10. A counter according to claim 9 wherein the said pulses determining the said gating period are applied to the said resistor via an inverter.

11. An electronic counter substantially as herein described with reference to the



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5 accompanying drawings.

12. A telecommunications receiver including a counter according to any of the 5 preceding claims arranged to provide a digital indication of the frequency of oscillations therein.

wherein the evaluation and display of the least significant place of the count of said frequency takes place in steps corresponding to frequency or channel spacing, in the waveband to which the receiver is tuned. 10

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13. A receiver according to claim 12

Printed for Her Majesty's Stationery Office by The Tweeddale Press Ltd., Berwick-upon-Tweed, 1978.
Published at the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.