CLAIMS

1. An integrated circuit, comprising:

a pixel, comprising:

a photodetection region; and

a drain configured to discard charge carriers from within a semiconductor region of the pixel outside of the photodetection region.

2. The integrated circuit of claim 1, wherein the drain is configured such that the drain does not extract charge carriers from the photodetection region when the drain is biased at a voltage in an operational voltage range of the pixel.

3. The integrated circuit of claim 1 or claim 2, wherein the drain is maintained at a fixed voltage.

4. The integrated circuit of any one of claims 1-3, wherein a voltage of the drain is variable.

5. The integrated circuit of any one of claims 1-4, wherein the drain comprises a semiconductor region.

6. The integrated circuit of claim 5, further comprising a conductive contact that contacts the semiconductor region.

7. The integrated circuit of claim 6, wherein the conductive contact is a metal plug.

8. The integrated circuit of claim 6 or claim 7, wherein the conductive contact does not extend outside an area of the drain in plan view.

9. The integrated circuit of claim 5, wherein the semiconductor region is doped.

10. The integrated circuit of claim 9, wherein the semiconductor region is n-type doped.

11. The integrated circuit of claim 10, further comprising a second semiconductor region that is p-type doped under the semiconductor region that is n-type doped.

12. The integrated circuit of any one of claims 1-11, wherein the semiconductor region is spaced apart from the photodetection region.

13. The integrated circuit of any one of claims 1-12, wherein the drain is a first drain and the pixel further comprises a second drain.

14. The integrated circuit of claim 13, wherein the first drain is on a first side of the photodetection region and the second drain is on a second side of the photodetection region.

15. The integrated circuit of claim 13 or claim 14, wherein the pixel further comprises a third drain.

16. The integrated circuit of claim 15, wherein the third drain is within a readout region of the pixel.

17. The integrated circuit of claim 15 or claim 16, wherein the third drain is configured to discard carriers from the photodetection region.

18. The integrated circuit of any one of claims 1-17, wherein the drain comprises a pn junction or a Schottky junction.

19. The integrated circuit of any one of claims 1-18, wherein the drain establishes a depletion region that overlaps with a depletion region of the photodetection region.

20. The integrated circuit of any one of claims 1-19, wherein the drain is configured to collect and discard charge carriers under pixel circuitry or one or more doped regions.

21. The integrated circuit of any one of claims 1-20, wherein the drain is a first drain and the integrated circuit further comprises a second drain, wherein the second drain is configured to discard carriers from the photodetection region.

~~22. An integrated circuit, comprising:~~

~~a pixel, comprising:~~

~~a photodetection region; and~~

a drain configured to discard charge carriers from the photodetection region, wherein the drain comprises a semiconductor region and the semiconductor region is contacted by a metal contact.

23. The integrated circuit of claim 22, wherein the semiconductor region is in contact with the photodetection region.

24. The integrated circuit of claim 22 or claim 23, wherein the semiconductor region is doped.

25. The integrated circuit of claim 24, wherein the semiconductor region is separated from a photodetection region by a second semiconductor region of opposite doping type from that of the semiconductor region.

26. The integrated circuit of any one of claims 22-25, wherein the drain is controlled to be at a first voltage when the drain pulls charge carriers out of the photodetection region and is controlled to be at a second voltage when the drain does not pull charge carriers out of the photodetection region.

27. The integrated circuit of any one of claims 22-26, wherein the drain is configured to produce a potential barrier between the photodetection region and the drain when the drain does not discard charge carriers from the photodetection region.

28. The integrated circuit of any one of claims 22-27, wherein the metal contact does not extend outside an area of the drain in plan view.

29. The integrated circuit of any one of claims 22-28, further comprising a silicide material between the metal contact and the drain.

30. The integrated circuit of any one of claims 22-29, wherein there is no polysilicon in an electrical path between the metal contact and the drain.

31. An integrated circuit, comprising:

a pixel, comprising:

a photodetection region; and

a drain configured to discard charge carriers from the photodetection region, wherein the drain comprises a semiconductor region that to which electrical contact is made through a conductive path that does not include a polysilicon electrode.

32. The integrated circuit of claim 31, wherein the semiconductor region is in contact with the photodetection region.

33. The integrated circuit of claim 31 or claim 32, wherein the semiconductor region is doped.

34. The integrated circuit of claim 33, wherein the semiconductor region is separated from a photodetection region by a second semiconductor region of opposite doping type from that of the semiconductor region.

35. The integrated circuit of any one of claims 31-34, wherein the drain is controlled to be at a first voltage when the drain pulls charge carriers out of the photodetection region and is controlled to be at a second voltage when the drain does not pull charge carriers out of the photodetection region.

36. The integrated circuit of any one of claims 31-35, wherein the drain is configured to produce a potential barrier between the photodetection region and the drain when the drain does not discard charge carriers from the photodetection region.

37. The integrated circuit of any one of claims 31-36, wherein the electrical contact is made by a metal contact that does not extend outside an area of the drain in plan view.

38. An integrated circuit, comprising:

a pixel, comprising:

a photodetection region; and

a photodiode configured to collect and drain unwanted charge carriers.

39. The integrated circuit of claim 38, wherein the photodiode is a first photodiode and the photodetection region comprises a second photodiode.

~~40. The integrated circuit of claim 39, wherein the first and second photodiodes have a same doping profile.~~

~~41. The integrated circuit of claim 39 or claim 40, wherein the first and second photodiodes are pinned photodiodes.~~

~~42. The integrated circuit of any one of claims 38-41, wherein the photodetection region comprises a gate to transfer charge carriers from the photodetection region to a charge storage region.~~

~~43. The integrated circuit of any one of claims 38-42, wherein the photodetection region is a first photodetection region and the photodiode is between the first photodetection region and a second photodetection region.~~

~~44. The integrated circuit of claim 43, wherein the photodiode is configured to collect and drain unwanted charge carriers from between the first and second photodetection regions.~~

~~45~~22. A method of manufacturing an integrated circuit, the method comprising:

forming a pixel comprising a photodetection region and a drain configured to discard charge carriers from within a semiconductor region of the pixel outside of the photodetection region.

~~46. A method of manufacturing an integrated circuit, the method comprising:~~

~~forming a pixel comprising a photodetection region and a drain configured to discard charge carriers from the photodetection region; and~~

~~forming a metal contact contacting the drain.~~

~~47. A method of manufacturing an integrated circuit, the method comprising:~~

~~forming a pixel comprising a photodetection region and a drain configured to discard charge carriers from the photodetection region; and~~

~~electrically contacting the drain through a conductive path that does not include a polysilicon electrode.~~

~~48. A method of manufacturing an integrated circuit, the method comprising:~~

~~forming a pixel comprising a photodetection region and a photodiode configured to collect and drain unwanted charge carriers.~~