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CIRCUITS WITH NEGATIVE DIFFERENTIAL RESISTANCE CHARACTERISTICS

Technical Field

5 This invention relates to circuits with negative differential resistance characteristics and refers particularly, though not exclusively, to a semiconductor device including circuits with negative differential resistance characteristics.

10 Background

It is known to use an operational amplifier ("opamp") to produce negative resistance characteristics where $R_{IN} = -R_{NF} (R_1/R_2)$. An opamp is an analog device having a low leakage in the range of about 5.4 to 20 μ A. The offset from the ground is 4 to 20mV and has a quiescent current of about 5– 8mA. The frequency response is normally about 200MHz. An opamp has a number of stages and a relatively high number of transistors. This limits the frequency response. Also, there is input leakage, and an offset voltage is created on the inputs and the vertical ground. The quiescent current is relatively high.

20 Summary

According to an exemplary aspect there is provided a circuit with negative differential resistance characteristics. The circuit comprises a first transistor with a first transistor gate, a first transistor source and a first transistor drain; a second transistor with a second transistor gate, a second transistor source and

a second transistor drain; and a third transistor with a third transistor gate, a third transistor source and a third transistor drain. The third transistor drain is operatively connected to the first transistor gate and the second transistor gate. The third transistor is operatively connected to the second transistor. There is a
5 first feedback loop to the gate of the first transistor and a second feedback loop to the gate of the second transistor.

The circuit may further comprise a first source for a first variable voltage operatively connected to the third transistor source.
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The circuit may further comprise a second source for a current operatively connected to the second transistor source.

The circuit may further comprise a current drain operatively connected to the
15 second transistor source.

The first transistor gate and the second transistor gate may be operatively connected to form a current mirror pair. The first feedback loop and the second feedback loop may be the same loop. The first feedback loop may be from the
20 drain of the third transistor. The second feedback loop may be from the drain of the third transistor.

The third transistor drain may be operatively connected to the second transistor drain. The first transistor drain may be operatively connected to the third transistor gate.

- 5 The circuit may further comprise an input operatively connected to the operative connection between the first transistor drain and the third transistor gate. The input may be able to have operatively connected thereto an input power supply for providing an input voltage to the operative connection between the first transistor drain and the third transistor gate. At least one biasing resistor may
- 10 be provided in the input. At least one second biasing resistor may be operatively connected between the input and the biasing power supply.

- The circuit may further comprise an output for voltage. The output may comprise an output transistor and a load resistor operatively connected to the
- 15 output transistor. The output for voltage may be operatively connected across the third transistor.

- The circuit may further comprise a fourth transistor with a fourth transistor gate, a fourth transistor source and a fourth transistor drain; and a fifth transistor with
- 20 a fifth transistor gate, a fifth transistor source and a fifth transistor drain. The fourth transistor source may be operatively connected to the third transistor drain. The second transistor source and the second transistor gate may be operatively connected to the fourth transistor. The second transistor source and the second transistor gate may be operatively connected to the fourth transistor

source. The second transistor source and the second transistor gate may be operatively connected to the fourth transistor drain. The fourth transistor gate may be operatively connected to the fifth transistor drain and a sixth transistor source. The fifth transistor gate and the sixth transistor gate may be operatively
5 connected to the first source for a first variable voltage.

The first feedback loop may be operatively connected from the fourth transistor source to the first transistor gate. The fourth transistor gate may be operatively connected to the first transistor gate. The second feedback loop may be
10 operatively connected from the fourth transistor drain to the second transistor gate.

The fifth transistor source may be operatively connected to the fourth transistor source. The fifth transistor drain may be operatively connected to the fourth
15 transistor drain and the second transistor source. The fifth transistor drain may be operatively connected to the second transistor drain. The fifth transistor gate may be operatively connected to a second source of a voltage.

The circuit may further comprise a third source of a variable voltage operatively
20 connected to the first transistor drain and the second transistor drain, and to the first source of a first variable voltage. The first variable voltage may be positive and the second variable voltage may be negative.

The circuit may be used for a purpose selected from: mixing, frequency doubling, phase reversal modulation, amplitude modulation, selective amplification, UJT device, application-relaxation oscillator, SCR triggering circuits, and suppression of amplification of an input signal.

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Brief Description of the Drawings

In order that the invention may be better understood and readily put into practical effect, exemplary embodiments shall now be described by way of non-limitative example only, the description being with reference to the accompanying illustrative
10 drawings.

In the drawings:

Figure 1 is a diagram of a prior art PMOS transistor and a graph of its current vs gate voltage;

Figure 2 is (a) a circuit diagram of an exemplary circuit and (b) a graph of its
15 current vs input voltage;

Figure 3 is (a) a circuit of an exemplary embodiment being a combination of the circuits of Figures 1 and 2, (b) a graph of its current vs input voltage, (c) a computer simulation of the circuit of (a), (d) a graph of the current vs voltage for the circuit of (c), and (e) to (i) are graphs of current vs voltage for different levels
20 of V_3 ;

Figure 4 is (a) an illustration of another exemplary embodiment and (b), (c) and (d) are graphs of its current vs input voltage;

Figure 5 is (a) a computer simulation of the circuit of Figure 4(a) and (b), (c) and (d) are graphs of its current vs voltage;

Figure 6 is (a) an illustration of a further exemplary embodiment and (b), (c) and (d) are graphs of its current vs input voltage;

Figure 7 is (a) a computer simulation of the circuit of Figure 6(a) and (b), (c) and (d) are graphs of its current vs voltage;

- 5 Figure 8 is (a) an illustration of yet another exemplary embodiment and (b) and (c) are graphs of its current vs input voltage;

Figure 9 is (a) a computer simulation of the circuit of Figure 8(a) and (b), (c) and (d) are graphs of its current vs voltage;

- Figure 10 is (a) an illustration of a more complex exemplary embodiment and
10 (b) and (c) are graphs of its current vs input voltage;

Figure 11 is (a) a computer simulation of the circuit of Figure 10(a) and (b), (c) and (d) are graphs of its current vs voltage;

Figure 12 is (a) an illustration of another exemplary embodiment and (b) and (c) are graphs of its current vs input voltage;

- 15 Figure 13 is (a) a computer simulation of the circuit of Figure 12(a) and (b) to (f) are graphs of its current vs voltage;

Figure 14 is (a) an illustration of another exemplary embodiment and (b), (c) and (d) are graphs of its current vs input voltage;

- Figure 15 is (a) a computer simulation of the circuit of Figure 14(a) and (b), (c)
20 and (d) are graphs of its current vs voltage;

Figure 16 is (a) an illustration of another exemplary embodiment and (b), (c) and (d) are graphs of its current vs input voltage;

Figure 17 is (a) a computer simulation of the circuit of Figure 16(a) and (b), (c) and (d) are graphs of its current vs voltage;

Figure 18 is (a) an illustration of a quadrant 2 circuit similar to the quadrant 1 circuit of Figure 3, and (b) and (c) are graphs of its current vs input voltage;

Figure 19 is (a) a computer simulation of the circuit of Figure 18(a) and (b) is a graph of its current vs voltage;

- 5 Figure 20 is (a) an illustration of a final exemplary embodiment and (b) and (c) are graphs of its current vs input voltage;

Figure 21 is (a) a computer simulation of the circuit of Figure 20(a) and (b) is a graph of its current vs voltage;

- Figure 22 is (a) another computer simulation of the circuit of Figure 21(a) and
10 (b) and (c) are graphs of its current vs voltage; and

Figure 23 is (a) a circuit that is a variant of that of Figure 3, with (b) and (c) being graphs of current vs voltage, and (d) being a graph of V_{OUT} vs V_{IN} .

15 Detailed Description of Exemplary Embodiments

- In Figure 1 there is shown a PMOS transistor Q3 operating in quadrant 1. The input is to the gate of Q3. When the input voltage V_{IN} is low, the transistor Q3 is strongly on with high source/drain current. When the input voltage V_{IN} is high, the transistor Q3 is shut off and the source/drain current is zero. As such
20 transistor Q3 exhibits a strong negative differential resistance characteristic as the current decreases with increasing voltage.

For Figure 2(a), there are two PMOS transistors – Q1 and Q2 with the input voltage being applied to the gate of both transistors Q1 and Q2, the gates also

being operatively connected to form a current mirror pair. . The output is shown in Figure 2(b). When $V_{IN} = 0$, the current I_{Q1} is linearly dependent on V_{IN} for a fixed gate/source voltage, VGS, curve. The VGS curve is controlled to a certain extent by a high value of the currents I_{Q2} or I_{Q3} . The values of I_{Q2} and I_{Q3} do not change significantly in the initial portion of the curve – that portion starting from $V_{IN} = 0$.

Figure 3 (a) is a combination of the circuits of Figures 1 and 2. As can be seen, the V_{cc} is now applied to the source of transistor Q3. In addition, the input voltage V_{IN} is applied to the gate of transistor Q3 and drain of transistor Q1. The output from transistor Q3 is the input to the gates of transistors Q1 and Q2 and to the drain of transistor Q2. The transistors Q1 and Q2 form a current mirror pair. The output current (I_{IN}) is shown in Figure 3 (b). By having the input to the gate of transistor Q3 (i.e. no DC current) and using the drain current of transistor Q3 to provide feedback to generate the impact response current I_N , I_N rises from zero to a peak and then falls to zero again as V_{IN} rises from 0v to V_{cc} , when transistor Q3 switches to off.

The nature of the feedback allows a rapid response. It also provides both positive and negative differential resistance characteristics over part of the input voltage range. By using P type CMOS transistors, the circuit of Figure 3(a) can be integrated into CMOS designs during the fabrication process.

By having V_{cc} a variable power supply or parameter to this device, the current vs voltage curve changes as V_{cc} increases and decreases. As such there is a family of current vs voltage curves with V_{cc} as a parameter. The current flow is governed by Q3. As V_{cc} increases the slope is more negative. But as V_{cc} decreases, the slope is less negative on the negative resistance portion of the curve. Since the circuit total current is governed by I_{Q3max} and I_{Q3max} is governed by the W/L ratio of Q3, when V_{IN} is 0V. and V_{cc} is 0V., Q3 is at 0V. As such, the V_{cc} supply can be varied appropriately to provide the required frequency response. V_{cc} may be supplied from an operational amplifier, another transistor, or a bias resistor as required or desired. The frequency response may be in the RF range of 500 KHz to 300 GHz. The circuit of Figure 3(a) may be used for functions such as, for example, mixing, frequency doubling, phase reversal modulation, amplitude modulation, selective amplification, UJT device, application–relaxation oscillator, SCR triggering circuits, and suppression of amplification of an input signal may be able to be achieved. This may be by use of terminals T1, T2 and T3.

It has positive and negative resistance characteristics. The terminal T1 has its input and output shared. Therefore the feedback path going forwards and backwards are the same. Also, the circuit has positive and negative Feedback at the same time. Therefore it can be stable in the negative resistance portion of its transfer characteristics. The feedback (feedforward) path has voltage to current (negative) through Q3 and current to voltage (Q2) and voltage to current (Q1) feedback (feedforward).

In addition, the circuit has two cut off points - at a low V_{cc} and at a high V_{cc} .

At the positive resistance portion of the current vs voltage curve the T1 shared input and output has negative feedback from Q1.

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Figure 3(c) is a computer simulation of the circuit of Figure 3(a). Here, M1 is Q1, M3 is Q2, M4 is Q3 and V3 is V_{cc} . Figure 3(d) shows the I vs V curve when V3 is 10V. In Figures 3(e) to (i) V3 (i.e. V_{cc}) is changed to 8V, 9V, 10V, 11V and 12V respectively. The resultant increase in the maximum current of the curve is clearly shown. This established that the maximum current is dependent on V_{cc} (V3).

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The circuit of Figures 3(a) and (c) has the advantages that there is a power supply V_{cc} to provide bias so as to be able to control the I vs V curve, and an additional terminal or terminals to derive related signals.

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As shown in Figures 23 (a) and (d) the use of the current mirror pair Q1 and Q2 allows for a separate output V_{OUT} . The graph of V_{OUT} vs V_{IN} is shown in Figure 23(d). R3 is a load resistor for the output transistor Q4, the resistor R3 and transistor Q4 being operatively connected across transistor Q3. The amplifier of output transistor Q4 and R3 is the simplest way to have the output V_{OUT} . If the transistors are sized such that the width of transistor Q4 is, for example, five times that of transistor Q2 then there is five times the current gain. So it is possible to have both current gain and, through Q4/R3, voltage amplification.

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Furthermore, and as shown in Figure 23(a), resistive bias may be added to modify the behavior of the circuit. This may be by adding R1 and/or R2. R1 may be used to adjust the characteristics of the I vs V curve as shown in Figure 23(a) and (b), with Figure 23 (b) showing the curve with R1 added. This shows that the curve is a superposition of the curves of R1, and that of the circuit of Figure 3(a). If R2 is of the correct value, R2 together with the circuit of Figure 3(a) under the source excitation V_{IN} will be a negative resistance amplifier. That amplification is able to be captured by the Q4/R3 amplifier. This may be with R1 removed.

The use of the current mirror pair Q1 and Q2 also allows for scaling up. It also provides the mirrored current on the negative resistance side that can be scaled up or down. As will be clear from the following description, by using current sources and/or drains it is possible to modify the I vs V curve. The current sources and/or drains can be integrated on the same IC.

The three transistors Q1, Q2 and Q3 may be NMOS, PMOS, or both N or P MOS i.e. CMOS device combinations.

Furthermore, if a resistive bias is applied to a different terminal, signals may be applied to other terminals to achieve modulation of the input signals.

If the circuit is used as an amplifier, the additional mirrored current and the signal can be tapped for further modification without loading the two-terminal circuit. This may be by use of an additional mirror transistor.

- 5 In Figure 4 the same circuit as Figure 3(a) is used with the addition of a current source I_2 operatively connected to the drain of transistor Q2 and the gates of transistors Q1 and Q2. V_{cc} is operatively connected to the source of transistor Q3 as indicated, and as per the exemplary embodiment of Figure 3. When V_{IN} is low, the gate/source voltage V_{GS} of Q2 is high due to I_2 . Although the
- 10 drain/source voltage V_{DS} of Q1 controls the current, the gain is higher due the gate/source voltage V_{GS} of Q1 and Q2. When V_{IN} is high, Q3 cuts off, but as Q2 still has current I_2 , as does Q1, this sets the current flowing in Q1 at a matching level of I_2 (Figure 4(c)). The slope of the negative resistance portion can be lowered by adjusting the transistor width parameter W of Q1. Therefore, and in
- 15 a similar manner to the exemplary embodiment of Figure 3, a family of curves can be obtained by varying I_2 as is shown in Figure 4(d).

- Figure 5(a) is a computer simulation of the circuit of Figure 4(a). Here, M1 is Q1, M3 is Q2, M4 is Q3, V3 is V_{cc} and XMM1 measures the current through I_2 .
- 20 V5, I1 together make I_2 . Figure 5(b) shows the I vs V curve when V3 is 10V and I_2 is 51.514 μA . In Figures 5(c) and (d) I_2 is changed to 101.252 μA and 202.505 μA respectively. The resultant increase in the current of the end of the curve is clearly shown. This established that the final current is dependent on I_2 .

Figure 6 shows a similar circuit to that of Figure 3 except that the current source I_2 is replaced by a current sink I_2 to ground. When V_{IN} is low, Q3 is strongly on (Figure 6(b)). However, the gate/source voltage V_{GS} of Q2 is low until the current in Q3 exceeds the sink current I_2 . Then, the gate/source voltage V_{GS} of Q2 increases. Current will then start to flow in Q1, corresponding to $I_{Q3} = I_2$ (Figure 6(c)). By using the sink current I_2 as a parameter, a family of current vs voltage curves can be obtained as shown in Figure 6(d). The current sink ceases to be a current sink when $I_2 = 0$ and thus it works as a current sink only in the quadrant 1 region.

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Due to feedback, the distance between the start of the three current vs voltage curves is quite small and the three curves start quite close together - they all start at or very close to the origin.

15 Figure 7(a) is a computer simulation of the circuit of Figure 6(a). Here, M1 is Q1, M3 is Q2, M4 is Q3, V3 is V_{cc} and V5, M2 make up I_2 . XMM1 measures the current through I_2 or M2. Figure 7(b) shows the I vs V curve when V3 is 10V and I_2 is 0 μA . In Figures 7(c) and (d), I_2 is changed to 51.686 μA and 203.482 μA respectively. The resultant decrease in the maximum current of the peak of the curve is clearly shown. This established that the final current is dependent on I_2 .

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In Figure 8 there is shown the circuit of the exemplary embodiment of Figure 3 combined with a similar circuit to give a V_{cc} dependent current sink. Three extra

transistors – Q4, Q5 and Q6 – are provided with the drain of Q4 being operatively connected to the drain of Q3 as well as the gates of Q1 and Q2. The gate of Q4, is operatively connected to the source of Q5 and the drain of Q6 with the source of Q6 being operatively grounded and the drain of Q5 at V_{cc} . V_{cc} is also operatively connected to the gates of Q5 and Q6. Q5 and Q6 have a ratio such that they produce a transfer characteristic to drive Q4 as a voltage-controlled current sink. With V_{cc} set at V_{ccmax} , V_S is set at the $\gg V_t$ of Q4. When V_{cc} decreases, V_S decreases Q4 will sink a current determined by the gate/source voltage V_{GS} of Q4.

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As is shown in Figure 8(c) a family of curves is obtained by varying V_{cc} . It is possible to increase V_{cc} to above V_{CCmax} , but the family of curves will be governed by I_{Q3max} and the new V_{cc} value.

15 Figure 9(a) is a computer simulation of the circuit of Figure 8(a). Here, M1 is Q1, M3 is Q2, M4 is Q3, M2 is Q4, M5 is Q5, M6 is Q6, V3 is V_{cc} , V5 is V_S and XMM1 measures the current through I2, the current sink. Figure 9(b) shows the I vs V curve when V3 (V_{cc}) is 10V and V_S (V5) is 10V. In Figures 9(c) and (d), V3 (V_{cc}) is changed to 8V and 5V respectively. The resultant decrease in the
20 maximum current of the peak of the curve is clearly shown. This establishes that the current is dependent on V_{cc} .

Figure 10 shows another quadrant 1 device where two further transistors – Q4 and Q5 - are added to the exemplary embodiment of Figure 3 between Q3 and

Q2. The drain of Q4 is operatively connected to the drain of Q3 and the feedback line is operatively connected from the drain of Q4 to the gates of Q4 and Q1. The gate of Q4 is operatively connected to the gate of Q1, the gates of Q1 and Q2 not being operatively connected. The drain and gate of Q2 are

5 operatively connected to the source of Q4. The drain of Q5 is operatively connected to the drain of Q4, and the source of Q5 is operatively connected to the source of Q4 and the drain of Q2. The gate of Q5 is operatively connected to V_p . Q2 and Q4 should have the same W/L ratio. Q1 is driven by twice the gate/source voltage V_{GS} of Q2 and Q4. The current through Q2 and Q4 will be

10 the same when Q5 is off. This establishes the upper limit of $2xI_{Q3max}$. When Q5 is switched on, it shorts out Q4 thus leaving only Q2 to bias the gate of Q1. This establishes the lower limit of I_{Q3max} . Driving V_{p1} such that Q5 is between fully on and fully off will result in current vs voltage curves between those limits. It is possible to add even more transistors to Q2 and Q4 to further increase the

15 slope to $3xI_{Q3max}$, or more. The maximum limit is determined by the maximum of I_{Q1} as well as the gate/source voltage V_{GS} and drain/source voltage V_{DS} of Q1. It is also limited by I_{Q3} and the voltage headroom of Q3. This is shown in Figures 10(b) and (c).

20 Figure 11(a) is a computer simulation of the circuit of Figure 10(a). Here, M1 is Q1, M3 is Q2, M4 is Q3, M2 is Q4, M5 is Q5, V3 is V_{cc} and V5 is V_{P1} . Figure 11(b) shows the I vs V curve when V3 is 10.1V and V5 (V_{P1}) is 4.5V. In Figure 11(c) and (d), V5 (V_{P1}) is changed to 7.5V and 12V respectively. The resultant decrease in the maximum current of the peak of the curve, and the operation in

the first two quadrants, is clearly shown. This establishes that the current is dependent on V_{P1} . In Figures 11(b), (c) and (d) the X-axis has been moved down two units to show the match with Figure 10 and to keep the same scale.

- 5 The circuit of Figure 12 is the same as that of Figure 10 except that the source of Q5 is operatively connected to the source of Q2 rather than the drain of Q2. This will allow a more dynamic control. With Q5 off, the circuit will operate as described with reference to Figure 10. With Q5 fully on, it will generate a drain/source voltage V_{DS} of Q5. If the V_{DS} of Q5 is below the V_t of Q1, the circuit
10 is off. With Q5 partially on, it will shunt the I_{Q3} current. This will again produce a family of curves, as shown in Figure 12(c).

- Figure 13(a) is a computer simulation of the circuit of Figure 12(a). Here, M1 is Q1, M3 is Q2, M4 is Q3, M2 is Q4, M5 is Q5, V3 is V_{cc} and V5 is V_{P1} . Figure
15 13(b) shows the I vs V curve when V3 is 10V and V5 (V_{P1}) is 0V. In Figure 13(c) to (f), V5 (V_{P1}) is changed to 2V, 4V, 6V and 8V respectively. The resultant decrease in the maximum current of the peak of the curve, and the operation in the first two quadrants is clearly shown. The current decreases as V_{P1} approaches V_{cc} . This establishes that the current is dependent on V_{P1} .

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In Figure 14(a), the circuit is similar to that of Figure 3 but an extra, negative variable voltage source $-V_{CC2}$ is added. Figure 14(b) is where $V_{CC2} = 0$ and $-V_{cc1}$ is 10V. If $-V_{CC2}$ is of a value the same as V_{CC} , Figure 14(c) is the result. V_{CC2}

can be adjusted to be of a value slightly less than V_{cc} (-4V vs 6V) and Figure 9(d) is the result with the curve being centred on the I axis. This may be combined with a current source to shift the curve downwardly, or a current sink to shift the curve upwardly. Therefore, by appropriate selection of V_{cc} , V_{cc2} , a
 5 current source, and current drain, the circuit may operate in any one of the four quadrants.

Figure 15(a) is a computer simulation of the circuit of Figure 12(a). Here, M1 is Q1, M3 is Q2, M4 is Q3, V3 is V_{cc2} and V5 is V_{cc1} . Figure 15(b) shows the I vs V
 10 curve when V3 is 10V and V5 (V_{cc}) is 0V. The curve starts at the origin. In Figure 15(c) V5 and V3 are both 5V. The curve is moved along the V axis to the left so the circuit is operating in the fourth and first quadrants. In Figure 15(d), V5 is 6V and V3 is 4V. The curve is centred on the I axis.

15 The addition of the current source I_N to the circuit of Figure 14(a) is shown in Figure 16. As is expected from Figures 4 and 5, the addition of the current source I_N at T1 can be used to raise or lower the curve depending on I_N being a current source (Figure 16(c)) or a current sink (Figure 16(d)).

20 Figure 17(a) is a computer simulation of the circuit of Figure 16(a). Here, M1 is Q1, M3 is Q2, M4 is Q3, V3 is $-V_{cc2}$, V6 is V_{cc1} , and XMM1 is I_N . Figure 17(b) shows the I vs V curve when V3 is 7V, V6 is 10.1V and I_N is 1.776 μ A. In Figure 17(c) I_N is changed to 150.990 μ A and in Figure 17(d) it is 250.000 μ A.

The same modifications may be made to similar circuits that operate in the second, third and fourth quadrants.

Figure 18 shows a circuit similar to that of Figure 3 but operating in the second quadrant. Its current vs voltage curve is shown in Figure 18(b). Figure 18(c) shows the curves after the circuit is modified by adding a V_{CC1} , V_{CC2} , and a current source.

Figure 19(a) is a computer simulation of the circuit of Figure 18(a) and Figure 19(b) shows the I vs V curve when V_3 is 10.1V and V_2 is 5V.

Figure 20(a) shows a circuit similar to Figure 3 but with a second mirror transistor pair Q_4 and Q_5 added. If Q_1 and Q_2 are matched, and Q_4 and Q_5 are matched, the I vs V curve is as shown in Figure 20(b). By scaling up the transistor sizes it is possible to increase the current gain on the I vs V characteristics on I_{in} vs V_{in} . Current gain can be used to transfer the operating point to the right hand side, with the operating voltage on the left hand side. This will apply to both the positive resistance region, as well as the negative resistance region. All of the gain and curve adjustment techniques discussed above may equally be applied here, as is shown in Figure 22.

Figure 21(a) is a computer simulation of the circuit of Figure 20(a). Here, M_1 is Q_1 , M_3 is Q_2 , M_4 is Q_3 , M_2 is Q_5 and M_5 is Q_4 . Figure 21(b) shows the I vs V

curve. In Figure 22 a second current measurement setup XSC2 is added to show the matching current flows, as is shown in Figures 22 (b) and (c).

Whilst there has been described in the foregoing description exemplary
5 embodiments it will be understood by those skilled in the technology concerned that many variations or modifications in details of design, construction and operation may be made without departing from the invention as defined in the following claims.

The Claims:

1. A circuit with negative differential resistances characteristics, the circuit comprising:
 - a first transistor with a first transistor gate, a first transistor source and a first transistor drain;
 - a second transistor with a second transistor gate, a second transistor source and a second transistor drain;
 - a third transistor with a third transistor gate, a third transistor source and a third transistor drain;
 - the third transistor drain being operatively connected to the first transistor gate and the second transistor gate;
 - the third transistor being operatively connected to the second transistor;
 - a first feedback loop to the gate of the first transistor; and
 - a second feedback loop to the gate of the second transistor.
2. A circuit as claimed in claim 1 further comprising a first source for a first variable voltage operatively connected to the third transistor source.
3. A circuit as claimed in claim 1 or claim 2 further comprising a second source for a current operatively connected to the second transistor source.
4. A circuit as claimed in claim 1 or claim 2 further comprising a current drain operatively connected to the second transistor source.
5. A circuit as claimed in any one of claims 1 to 4, wherein the first transistor gate and the second transistor gate are operatively connected to form a current mirror pair.

6. A circuit as claimed in claim 5, wherein the first feedback loop and the second feedback loop are the same loop.
7. A circuit as claimed in any one of claims 1 to 6, wherein the first feedback loop is from the drain of the third transistor.
- 5 8. A circuit as claimed in claim 7, wherein the second feedback loop is from the drain of the third transistor.
9. A circuit as claimed in any one of claims 1 to 8, wherein the third transistor drain is operatively connected to the second transistor drain.
- 10 10. A circuit as claimed in any one of claims 1 to 9, wherein the first transistor drain is operatively connected to the third transistor gate.
11. A circuit as claimed in claim 10 further comprising an input operatively connected to the operative connection between the first transistor drain and the third transistor gate.
12. A circuit as claimed in claim 11, wherein the input is able to have
15 operatively connected thereto an input power supply for providing an input voltage to the operative connection between the first transistor drain and the third transistor gate.
13. A circuit as claimed in claim 11 or claim 12, wherein at least one biasing resistor is provided in the input.
- 20 14. A circuit as claimed in claim 12, wherein at least one second biasing resistor is operatively connected between the input and the biasing power supply.
15. A circuit as claimed in any one of claims 1 to 14 further comprising an output for voltage, the output comprising an output transistor and a load resistor

operatively connected to the output transistor, the output for voltage being operatively connected across the third transistor.

16. A circuit as claimed in any one of claims 1 to 4 further comprising a fourth transistor with a fourth transistor gate, a fourth transistor source and a fourth transistor drain; and a fifth transistor with a fifth transistor gate, a fifth transistor source and a fifth transistor drain; the fourth transistor source being operatively connected to the third transistor drain; and the second transistor source and the second transistor gate being operatively connected to the fourth transistor.

17. A circuit as claimed in claim 16, wherein the second transistor source and the second transistor gate are operatively connected to the fourth transistor source.

18. A circuit as claimed in claim 16, wherein the second transistor source and the second transistor gate are operatively connected to the fourth transistor drain.

19. A circuit as claimed in claim 16 or claim 17, wherein the fourth transistor gate is operatively connected to the fifth transistor drain and a sixth transistor source.

20. A circuit as claimed in claim 19, wherein the fifth transistor gate and the sixth transistor gate are operatively connected to the first source for a first variable voltage.

21. A circuit as claimed in claim 16 or claim 18, wherein the first feedback loop is operatively connected from the fourth transistor source to the first transistor gate; the fourth transistor gate being operatively connected to the first transistor gate.

22. A circuit as claimed in any one of claims 16, 18 or 21, wherein the second feedback loop is operatively connected from the fourth transistor drain to the second transistor gate.
23. A circuit as claimed in any one of claims 16, 18, 21 or 22, wherein the fifth transistor source is operatively connected to the fourth transistor source.
24. A circuit as claimed in claim 23, wherein the fifth transistor drain is operatively connected to the fourth transistor drain and the second transistor source.
25. A circuit as claimed in claim 23, wherein the fifth transistor drain is operatively connected to the second transistor drain.
26. A circuit as claimed in any one of claims 16, 18 or 21 to 25, wherein the fifth transistor gate is operatively connected to a second source of a voltage.
27. A circuit as claimed in any one of claims 1 to 26 further comprising a third source of a variable voltage operatively connected to the first transistor drain and the second transistor drain, and to the first source of a first variable voltage.
28. A circuit as claimed in claim 27, wherein the first variable voltage is positive and the second variable voltage is negative.
29. A circuit as claimed in any one of claims 1 to 28, wherein the circuit is used for a purpose selected from the group consisting of: mixing, frequency doubling, phase reversal modulation, amplitude modulation, selective amplification, UJT device, application-relaxation oscillator, SCR triggering circuits, and suppression of amplification of an input signal.