

Description

The invention relates to a method of detecting binary information from an output signal of a charge transfer device, which signal comprises a train of pulses, which device is used for temporarily storing or for delaying said binary information in the form of charge packets, the amplitude of said pulses being representative of the binary information and being compared, in a comparator circuit, with a reference signal derived from an output signal of a reference source.

The invention also relates to a device for carrying out the method in accordance with the invention.

A known such method is already utilized in existing circuit arrangements, for example the Texas Instruments TMS 3064 described on pages 221—225 of the book "Charge Coupled Devices and Systems" by the authors Howes, M. J. and Morgan, D. V. (Published by Wiley & Sons 1979). In accordance with the known method the comparator circuit determines whether the output signal of the charge transfer device is larger or smaller than the reference signal. In the first-mentioned case, for example, a logic "1" will be detected, whilst in the last-mentioned case this will be a "0".

As is known, charge transfer devices comprise an array of cells arranged in sequence, between which charge transfer is possible under the influence of suitable clock signals. It is also known that such charge transfer devices have the disadvantage that signal losses may occur during transfer. To compensate for these losses, it is proposed already in U.S. patent specification 4,185,324 to determine the logic level of a signal by comparison with the logic level of the preceding signal representing known data, means being present for adding an adjustment voltage to one of said signals. The signals are fed into a sense amplifier, the output of which is connected to the input of a D-flip-flop, said flip-flop being present during the initial state when a known marker bit appears in the data cell storing said preceding signal. The output of the flip-flop delivers the output signal and moreover controls the means for adding the adjustment voltage to one of the signals. In this way, signal losses may be compensated. In the Specification of the U.S. Patent 4,185,324, there is started from the assumption that the signal losses for both cells are nearly equal. However, during transfer of a charge packet from one cell to the following cell, a residual charge is left in the first-mentioned cell, so that, firstly, the charge packet being transferred decreases in magnitude and, secondly, the residual charge is added to the next charge packet. For example, when a charge transfer device is used as a digital shift register, a charge packet representing a logic "0" may be distorted by a charge packet which represents a logic "1" and which directly precedes the first-mentioned charge packet. When the known method is used it may happen that the second charge packet is

distorted to such an extent that a logic "1" is detected erroneously. It is obvious that a similar error may occur in the case of a logic "1" which follows a logic "0".

It is an object of the invention to mitigate the said disadvantage. To this end the method in accordance with the invention is characterized in that in order to generate the reference signal an auxiliary signal is added to the output signal of the reference source, which auxiliary signal is substantially proportional to the value of the last pulse detected.

By means of the method in accordance with the invention the reference signal is always adapted in such a way that a pulse distorted as a result of the previously described effect still yields the correct binary value upon detection. For carrying out the method in accordance with the invention it is advantageous to employ a device in accordance with the invention. This device is characterized in that it comprises first means for storing the value of the last pulse detected until the instant at which the next pulse is detected, an adder circuit for adding the auxiliary signal to the output signal of the reference source, and second means for deriving the auxiliary signal from the signal stored by the first means and applying said auxiliary signal to the adder circuit.

The invention will now be described in more detail with reference to the drawing, in which

Figure 1 shows an example of the output signal of the charge transfer device together with the corresponding reference signal employed with the known method.

Figure 2 shows an example of the output signal of the charge transfer device together with the corresponding reference signal employed when using a method in accordance with the invention, and

Figure 3 is the block diagram of a device for carrying out a method in accordance with the invention.

Figure 1 shows an example of the variation of the output signal V_s of the charge transfer device together with the corresponding reference signal V_{ref} used in the known method. The reference signal V_{ref} is independent of the output signal V_s of the charge transfer device. The pulses 1, 2, 3 ... 13 each represent binary information. For example, the pulses 1, 2, 3, 8, 9, 10 and 13 each represent a logic "0" and the pulses 4, 5, 6 and 7 a logic "1".

Each time that a transition occurs in the output signal V_s from a logic "0" to a logic "1" and vice versa the pulse appearing at said transition is distorted, as is the case for the pulses 4, 8, 11 and 12. For the pulses 11 and 12 the distortion is even so strong that a correct interpretation is unlikely when the known method is used. It will be appreciated that pulse 11 is a distorted "1" pulse, which has degenerated under the influence of preceding "0" pulses, whilst pulse 12 should have been a "0". Thus, the data smear effect mentioned in the introduction renders the known method unreliable.

The method in accordance with the invention

utilises a reference signal which depends on the amplitude of the last pulse detected.

Figure 2 again shows the variation of the output signal in the same way as in Figure 1, but now together with the variation of the associated reference signal V'_{ref} when using a method in accordance with the invention. Between the pulses 3 and 4 a transition from logic "0" to logic "1" level occurs, so that in accordance with the inventive method the reference signal V'_{ref} is raised after pulse 4. In the example of Figure 2 the difference between the reference signal V'_{ref} and the output signal V_h of an auxiliary charge transfer device CA (see Figure 3) is substantially proportional to the amplitude of the last pulse detected. After the pulse following a transition from logic "1" to logic "0" level the reference signal V'_{ref} is reduced in accordance with the inventive method, as is illustrated for pulse 8. The pulses 11 and 12 are now interpreted correctly despite their substantial distortion.

Figure 3 is the block diagram of a device for carrying out a method in accordance with the invention. The output signal V_s of the charge transfer device C is applied to a comparator circuit D and also to a sample-and-hold circuit SH, which is controlled in synchronism with the clock signal of the charge transfer device C. Thus, the sample-and-hold circuit SH delays the pulses of the output signal V_s for one period of said clock signal. The output signal of the sample-and-hold circuit SH, whose magnitude is equal to the amplitude of the last pulse detected, is applied to an adder circuit A as an auxiliary signal V_a via a weighting-factor or attenuator circuit WF, which adder circuit also receives the output signal V_h of the auxiliary charge transfer device CA. The output signal of the adder circuit A is applied to the comparator circuit D as a reference signal V'_{ref} , the output signal V_o of said comparator circuit containing binary information which is represented by the pulses of the output signal V_s of the charge transfer device C.

In order to obtain a suitable reference signal V'_{ref} , as is shown in Figure 2, the output signal V_h of the auxiliary charge transfer device should be so low that after addition to the auxiliary signal V_a a reference signal V'_{ref} is obtained which varies around a reference level M (see Figure 2) situated half-way between the amplitudes of the largest and the smallest pulses. For this purpose the auxiliary charge transfer device is driven with so-called "fat zeroes", that is charge packets whose levels are slightly above the logic "0" level.

Claims

1. A method of detecting binary information from an output signal of a charge transfer device, which signal comprises a train of pulses, which device is used for temporarily storing or for delaying said binary information in the form of charge packets, the amplitude of said pulses being representative of the binary information and being compared, in a comparator circuit with

a reference signal derived from an output signal (V_h) of a reference source characterized in that in order to generate the reference signal an auxiliary signal (V_a) is added to the output signal of the reference source, which auxiliary signal is substantially proportional to the value of the last pulse detected.

2. A device for carrying out the method as claimed in Claim 1, characterized in that said device comprises first means for storing the value of the last pulse detected until the instant at which the next pulse is detected, an adder circuit for adding the auxiliary signal to the output signal of the reference source, and second means for deriving the auxiliary signal from the signal stored by the first means and applying said auxiliary signal to the adder circuit.

3. A device as claimed in Claim 2, characterized in that the first means comprise a sample-and-hold circuit having an input and an output, the second means comprise an attenuator circuit, the reference source comprises an auxiliary charge transfer device, the input of the sample-and-hold circuit being connected to an output of the charge transfer device for receiving the output signal of the charge transfer device, the output of the sample-and-hold circuit being connected to a first input of the adder circuit via the attenuator circuit, a second input of the adder circuit being connected to the auxiliary charge transfer device for receiving the output signal of the auxiliary charge transfer device, and an output of the adder circuit being connected to an input of the comparator circuit.

Patentsprüche

1. Verfahren zum Detektieren binärer Information aus einem eine Impulsfolge aufweisenden Ausgangssignal einer Ladungsübertragungsanordnung, die zur einstweiligen Speicherung oder Verzögerung dieser binären Information in Form von Ladungspaketen benutzt wird, wobei die Amplitude dieser Impulse für die binäre Information repräsentativ ist und in einer Vergleichsschaltung mit einem von einem Ausgangssignal (V_h) einer Bezugsquelle abgeleiteten Bezugssignal verglichen wird, dadurch gekennzeichnet, dass zum Erzeugen des Bezugssignals dem Ausgangssignal der Bezugsquelle ein Hilfsignal (V_a) addiert wird, das im wesentlichen dem Wert des zuletzt detektierten Impulses proportional ist.

2. Anordnung zum Durchführen des Verfahrens nach Anspruch 1, dadurch gekennzeichnet, dass diese Anordnung erste Mittel aufweist zum Speichern des Wertes des zuletzt detektierten Impulses bis zu dem Zeitpunkt, an dem der nächste Impuls detektiert wird, weiterhin eine Addierschaltung zum Addieren des Hilfsignals zu dem Ausgangssignal der Bezugsquelle sowie zweite Mittel zum Ableiten des Hilfsignals aus dem durch die ersten Mittel gespeicherten Signal und zum Zuführen des Hilfsignals zu der Addierschaltung.

3. Anordnung nach Anspruch 2, dadurch



utilises a reference signal which depends on the amplitude of the last pulse detected.

Figure 2 again shows the variation of the output signal in the same way as in Figure 1, but now together with the variation of the associated reference signal V'_{ref} when using a method in accordance with the invention. Between the pulses 3 and 4 a transition from logic "0" to logic "1" level occurs, so that in accordance with the inventive method the reference signal V'_{ref} is raised after pulse 4. In the example of Figure 2 the difference between the reference signal V'_{ref} and the output signal V_n of an auxiliary charge transfer device CA (see Figure 3) is substantially proportional to the amplitude of the last pulse detected. After the pulse following a transition from logic "1" to logic "0" level the reference signal V'_{ref} is reduced in accordance with the inventive method, as is illustrated for pulse 8. The pulses 11 and 12 are now interpreted correctly despite their substantial distortion.

Figure 3 is the block diagram of a device for carrying out a method in accordance with the invention. The output signal V_s of the charge transfer device C is applied to a comparator circuit D and also to a sample-and-hold circuit SH, which is controlled in synchronism with the clock signal of the charge transfer device C. Thus, the sample-and-hold circuit SH delays the pulses of the output signal V_s for one period of said clock signal. The output signal of the sample-and-hold circuit SH, whose magnitude is equal to the amplitude of the last pulse detected, is applied to an adder circuit A as an auxiliary signal V_a via a weighting-factor or attenuator circuit WF, which adder circuit also receives the output signal V_n of the auxiliary charge transfer device CA. The output signal of the adder circuit A is applied to the comparator circuit D as a reference signal V'_{ref} , the output signal V_o of said comparator circuit containing binary information which is represented by the pulses of the output signal V_s of the charge transfer device C.

In order to obtain a suitable reference signal V'_{ref} , as is shown in Figure 2, the output signal V_n of the auxiliary charge transfer device should be so low that after addition to the auxiliary signal V_a a reference signal V'_{ref} is obtained which varies around a reference level M (see Figure 2) situated half-way between the amplitudes of the largest and the smallest pulses. For this purpose the auxiliary charge transfer device is driven with so-called "fat zeroes", that is charge packets whose levels are slightly above the logic "0" level.

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1. A method of detecting binary information from an output signal of a charge transfer device, which signal comprises a train of pulses, which device is used for temporarily storing or for delaying said binary information in the form of charge packets, the amplitude of said pulses being representative of the binary information and being compared, in a comparator circuit with

a reference signal derived from an output signal (V_n) of a reference source characterized in that in order to generate the reference signal an auxiliary signal (V_a) is added to the output signal of the reference source, which auxiliary signal is substantially proportional to the value of the last pulse detected.

2. A device for carrying out the method as claimed in Claim 1, characterized in that said device comprises first means for storing the value of the last pulse detected until the instant at which the next pulse is detected, an adder circuit for adding the auxiliary signal to the output signal of the reference source, and second means for deriving the auxiliary signal from the signal stored by the first means and applying said auxiliary signal to the adder circuit.

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Patentansprüche

1. Verfahren zum Detektieren binärer Information aus einem eine Impulsfolge aufweisenden Ausgangssignal einer Ladungsübertragungsanordnung, die zur einstweiligen Speicherung oder Verzögerung dieser binären Information in Form von Ladungspaketen benutzt wird, wobei die Amplitude dieser Impulse für die binäre Information repräsentativ ist und in einer Vergleichsschaltung mit einem von einem Ausgangssignal (V_n) einer Bezugsquelle abgeleiteten Bezugssignal verglichen wird, dadurch gekennzeichnet, dass zum Erzeugen des Bezugssignals dem Ausgangssignal der Bezugsquelle ein Hilfssignal (V_a) addiert wird, das im wesentlichen dem Wert des zuletzt detektierten Impulses proportional ist.

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3. Anordnung nach Anspruch 2, dadurch



gekennzeichnet, dass die ersten Mittel eine Abtast-und-Halteschaltung mit einem Eingang und einem Ausgang aufweisen, die zweiten Mittel eine Dämpfungsschaltung aufweisen, die Bezugs- uelle eine Hilfs ladungsübertragungsanordnung aufweist, wobei der Eingang der Abtast-und-Halteschaltung mit einem Ausgang der Ladungsübertragungsanordnung verbunden ist zum Erhalten des Ausgangssignals der Ladungsübertragungsanordnung, wobei der Ausgang der Abtast- und Halteschaltung über die Dämpfungsschaltung mit einem ersten Eingang der Addierschaltung verbunden ist, während zum Erhalten des Ausgangssignals der Hilfs ladungsübertragungsanordnung ein zweiter Eingang der Addierschaltung mit der Hilfs ladungsübertragungsanordnung und ein Ausgang der Addierschaltung mit einem Eingang der Vergleichs- schaltung verbunden ist.

Revendications

1. Procédé de détection d'information binaire, dans un signal de sortie d'un dispositif de transfert de charges, signal qui comporte un train d'impulsions, ledit dispositif étant utilisé pour le stockage temporaire ou le retardement de cette information binaire sous la forme de paquets de charges, l'amplitude desdites impulsions étant représentative de l'information binaire et étant comparée, dans un circuit comparateur, avec un signal de référence déduit d'un signal de sortie d'une source de référence, caractérisé en ce que, pour engendrer le signal de référence, un signal

auxiliaire est ajouté au signal de sortie de la source de référence, signal auxiliaire qui est sensiblement proportionnel à la valeur de la dernière impulsion détectée.

2. Dispositif pour la mise en oeuvre du procédé selon la revendication 1, caractérisé en ce qu'il comporte de premiers moyens pour stocker la valeur de la dernière impulsion détectée jusqu'à l'instant où est détectée l'impulsion suivante, un circuit additionneur pour ajouter le signal auxiliaire au signal de sortie de la source de référence et de seconds moyens pour déduire le signal auxiliaire du signal stocké dans les premiers moyens et pour appliquer ce signal auxiliaire au circuit additionneur.

3. Dispositif selon la revendication 2, caractérisé en ce que les premiers moyens comportent un circuit d'échantillonnage et de maintien muni d'une entrée et d'une sortie, en ce que les seconds moyens comportent un circuit atténuateur, en ce que la source de référence comporte un dispositif de transfert de charges auxiliaire, l'entrée du circuit d'échantillonnage et de maintien étant reliée à une sortie du dispositif de transfert de charges pour recevoir le signal de sortie du dispositif de transfert de charges, la sortie du circuit d'échantillonnage et de maintien étant reliée à travers le circuit atténuateur à une première entrée du circuit additionneur dont une seconde entrée est reliée au dispositif de transfert de charges auxiliaire pour recevoir le signal de sortie du dispositif de transfert de charges auxiliaire et dont une sortie est reliée à une entrée du circuit comparateur.

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