

BRIEF SUMMARY

[0004] This summary is provided to introduce a selection of concepts in a simplified form. These concepts are described in further detail in the detailed description of example embodiments of the disclosure below. This summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used to limit the scope of the claimed subject matter.

[0005] In some embodiments, the present disclosure includes a method of forming a semiconductor structure. A semiconductor-on-insulator (SOI) substrate is provided that includes a base substrate, a stressor layer above the base substrate comprising a crystallographically strained material, a surface semiconductor layer, and a dielectric layer disposed between the stressor layer and the surface semiconductor layer. Ions are implanted into or through at least a first region of the stressor layer without implanting ions into or through at least a second region of the stressor layer. An additional semiconductor material is formed on the surface semiconductor layer above the at least a first region of the stressor layer. The strain state in a first region of the surface semiconductor layer above the at least a first region of the stressor layer is altered. A trench structure is formed through the surface semiconductor layer and into at least a portion of the base substrate, and a strain state in a second region of the surface semiconductor layer above the at least a second region of the stressor layer is altered, such that the strain rate in the second region of the surface semiconductor layer differs from the strain rate in the first region of the surface semiconductor layer.

[0006] In additional embodiments, the present disclosure includes semiconductor structures that may be fabricated by methods as disclosed herein. For example, in some embodiments, the present disclosure includes a semiconductor structure comprising a base substrate, and at least first and second regions disposed above the substrate. The first region includes a substantially strain relaxed layer disposed on the base substrate, a dielectric layer disposed above the substantially strain relaxed layer on a side thereof opposite the base substrate, and a compressively strained surface semiconductor layer disposed above the dielectric layer. The second region includes a compressively strained layer disposed on the base substrate, a dielectric layer disposed above the compressively strained layer on a side thereof opposite the base substrate, and a tensilely strained surface semiconductor layer disposed above the dielectric layer. The first and second regions are laterally separated from one another by a dielectric isolation material.

CLAIMS

What is claimed is:

1. A method of forming a semiconductor structure, comprising:
providing a semiconductor-on-insulator (SOI) substrate, the SOI substrate including:
a base substrate;
a stressor layer above the base substrate comprising a crystallographically strained material;
a surface semiconductor layer; and
a dielectric layer disposed between the stressor layer and the surface semiconductor layer;
implanting ions into or through at least a first region of the stressor layer without implanting ions into or through at least a second region of the stressor layer;
forming an additional semiconductor material on the surface semiconductor layer above the at least a first region of the stressor layer;
altering a strain state in a first region of the surface semiconductor layer above the at least a first region of the stressor layer;
forming a trench structure through the surface semiconductor layer into at least a portion of the base substrate; and
altering a strain state in a second region of the surface semiconductor layer above the at least a second region of the stressor layer,
wherein altering the strain state in the second region of the surface semiconductor layer above the at least a second region of the stressor layer comprises causing the strain state in the second region of the surface semiconductor layer to differ from the strain state in the first region of the surface semiconductor layer.
2. The method of claim 1, wherein altering the strain state in the first region of the surface semiconductor layer comprises inducing compressive strain in the first region of the surface semiconductor layer.

3. The method of claim 1, wherein altering the strain state in the second region of the surface semiconductor layer comprises inducing tensile strain in the second region of the surface semiconductor layer.
4. The method of claim 1, wherein the stressor layer of the provided SOI substrate comprises a compressively strained $\text{Si}_x\text{Ge}_{1-x}$ layer.
5. The method of claim 1, wherein the dielectric layer of the provided SOI substrate comprises one or more dielectric layers, each dielectric layer comprising a material selected from the group consisting of silicon nitride, silicon oxide and silicon oxynitride.
6. The method of claim 1, wherein implanting ions into or through at least a portion of the stressor layer comprises implanting one or more of germanium, silicon, carbon, argon and inert gas ions into or through the at least a portion of the stressor layer.
7. The method of claim 1, wherein forming an additional semiconductor material on the surface semiconductor layer above the first region of the stressor layer further comprises epitaxially depositing $\text{Si}_{1-x}\text{Ge}_x$ on the surface semiconductor layer, the $\text{Si}_{1-x}\text{Ge}_x$ forming the additional semiconductor material.
8. The method of claim 1, wherein altering a strain state in a first region of the surface semiconductor layer above the at least a first region of the stressor layer further comprises diffusing elements from the additional semiconductor material into the first region of the surface semiconductor layer so as to increase a concentration of the diffused elements in the first region of the surface semiconductor layer.
9. A semiconductor structure, comprising:
a base substrate; and
at least a first region and a second region disposed above the base substrate;
wherein the first region includes:
a substantially relaxed layer disposed on the base substrate;

a dielectric layer disposed above the substantially relaxed layer on a side of the substantially relaxed layer opposite the base substrate; and
 a compressively strained surface semiconductor layer disposed above the dielectric layer;
 wherein the second region includes:
 a compressively strained layer disposed on the base substrate;
 a dielectric layer disposed above the compressively strained layer on a side thereof opposite the base substrate; and
 a tensilely strained surface semiconductor layer disposed above the dielectric layer; and
 wherein the first region and the second region are laterally separated from one another by a dielectric isolation material.

10. The semiconductor structure of claim 9, wherein the substantially relaxed layer of the first region comprises a substantially relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer.

11. The semiconductor structure of claim 9, wherein the compressively strained surface semiconductor layer of the first region comprises a compressively strained $\text{Si}_{1-y}\text{Ge}_y$ layer.

12. The semiconductor structure of claim 9, wherein the compressively strained layer of the second region comprises a compressively strained $\text{Si}_{1-x}\text{Ge}_x$ layer.

13. The semiconductor structure of claim 9, wherein the tensilely strained surface semiconductor layer of the second region comprises a tensilely strained silicon layer.

14. The semiconductor structure of claim 13, further comprising at least one device structure formed in the tensilely strained silicon layer.