CLAIMS

1. A data processing system for handling an input/output store instruction, the data processing system comprising:

a data processing unit including a core and system firmware, the data processing unit configured to perform a method, the method comprising:

identifying an input/output function by an address specified using the input/output store instruction, the input/output store instruction specifying at least the input/output function with an offset through the address, at least one of data to be transferred and a pointer to data to be transferred, and a length of the data;

verifying whether access to the input/output function is allowed on an address space and on a guest instance level;

completing the input/output store instruction before an execution of the input/output store instruction in a selected component of the data processing system different from the data processing unit is completed, the selected component configured to asynchronously load from and store data to at least one external device;

providing notification through an interrupt, based on detecting an error during an asynchronous execution of the input/output store instruction in the data processing unit, transmitting data of a failed asynchronous execution;

collecting a completion of the input/output store instruction and updating one or more input/output status buffers of multiple input/output status buffers based on received completion messages; and

delaying an execution of the input/output store instruction, until an input/output status buffer of the multiple input/output status buffers is available to store information about a completion of pending input/output store instructions.

2. The data processing system of claim 1, wherein the method further comprises delaying, by the data processing unit, an execution of at least one of an asynchronous input/output store instruction and a synchronous input/output store instruction, until an input/output status buffer

of the multiple input/output status buffers is available to store information about a completion of one or more pending input/output store instructions.

3. The data processing system of claim 1, wherein the selected component is a system nest communicatively coupled to the data processing unit via an aggregation buffer.

4. The data processing system of claim 3, wherein the data is transferred by the input/output store instruction through an asynchronous transmit mechanism with an early completion message in multiple data packets to the aggregation buffer, based on the length of the data exceeding a defined size.

5. The data processing system of claim 3, wherein the aggregation buffer is communicatively coupled to an asynchronous core-nest interface of the data processing unit, the asynchronous core-nest interface comprising an input/output status array including the multiple input/output status buffers.

6. The data processing system of claim 1, wherein the method further comprises collecting message states from the selected component, the message states comprising completion status from the selected component.

7. The data processing system of claim 6, wherein the message states are numbered by an input/output status buffer index.

8. The data processing system of claim 6, wherein the completion status is numbered by an input/output status buffer index.

9. The data processing system of claim 1, wherein the method further comprises collecting message states from an input/output bus controller coupled to the selected component, the message states comprising completion status from the selected component.

10. The data processing system of claim 1, wherein the data processing unit comprises an asynchronous core-nest interface, the asynchronous core-nest interface comprising an input/output status array including the multiple input/output status buffers to collect returned states from the selected component, the selected component being a system nest communicatively coupled to the data processing unit via an aggregation buffer and to at least one external device, the aggregation buffer being further communicatively coupled to the asynchronous core-nest interface.

11. The data processing system of claim 10, wherein the system firmware comprises an asynchronous input/output driver code to handle the input/output store instruction, and an array management logic to allocate and deallocate input/output status buffers in the input/output status array and to initiate a start of a new input/output store instruction.

12. The data processing system of claim 11, wherein the core comprises an asynchronous setup code to handle memory requirements for status information of the asynchronous input/output driver code.

13. The data processing system of claim 10, wherein the asynchronous core-nest interface comprises an asynchronous core-nest interface forwarding component to forward data with local completion.

14. The data processing system of claim 10, wherein the aggregation buffer comprises an early completion logic to deliver a free for reuse message after sending a request.

15. A computer program product for handling an input/output store instruction, the computer program product comprising:

at least one computer readable storage medium readable by at least one processing circuit and storing instructions for performing a method comprising:

identifying an input/output function by an address specified using the input/output store instruction, the input/output store instruction specifying at least the

input/output function with an offset through the address, at least one of data to be transferred and a pointer to data to be transferred, and a length of the data;

verifying whether access to the input/output function is allowed on an address space and on a guest instance level;

completing, by a data processing unit of a data processing system, the input/output store instruction before an execution of the input/output store instruction in a selected component of the data processing system different from the data processing unit is completed, the selected component configured to asynchronously load from and store data to at least one external device;

providing notification through an interrupt, based on detecting an error during an asynchronous execution of the input/output store instruction in the data processing unit, transmitting data of a failed asynchronous execution;

collecting a completion of the input/output store instruction and updating one or more input/output status buffers of multiple input/output status buffers based on received completion messages; and

delaying an execution of the input/output store instruction, until an input/output status buffer of the multiple input/output status buffers is available to store information about a completion of pending input/output store instructions.

16. The computer program product of claim 15, wherein the method further comprises delaying, by the data processing unit, an execution of at least one of an asynchronous input/output store instruction and a synchronous input/output store instruction, until an input/output status buffer of the multiple input/output status buffers is available to store information about a completion of one or more pending input/output store instructions.

17. The computer program product of claim 15, wherein the data processing unit comprises an asynchronous core-nest interface, the asynchronous core-nest interface comprising an input/output status array including the multiple input/output status buffers to collect returned states from the selected component, the selected component being a system nest communicatively coupled to the data processing unit via an aggregation buffer and to at least

one external device, the aggregation buffer being further communicatively coupled to the asynchronous core-nest interface.

18. A computer-implemented method of handling an input/output store instruction, the computer-implemented method comprising:

identifying an input/output function by an address specified using the input/output store instruction, the input/output store instruction specifying at least the input/output function with an offset through the address, at least one of data to be transferred and a pointer to data to be transferred, and a length of the data;

verifying whether access to the input/output function is allowed on an address space and on a guest instance level;

completing, by a data processing unit of a data processing system, the input/output store instruction before an execution of the input/output store instruction in a selected component of the data processing system different from the data processing unit is completed, the selected component configured to asynchronously load from and store data to at least one external device;

providing notification through an interrupt, based on detecting an error during an asynchronous execution of the input/output store instruction in the data processing unit, transmitting data of a failed asynchronous execution;

collecting a completion of the input/output store instruction and updating one or more input/output status buffers of multiple input/output status buffers based on received completion messages; and

delaying an execution of the input/output store instruction, until an input/output status buffer of the multiple input/output status buffers is available to store information about a completion of pending input/output store instructions.

19. The computer-implemented method of claim 18, further comprising delaying, by the data processing unit, an execution of at least one of an asynchronous input/output store instruction and a synchronous input/output store instruction, until an input/output status buffer of the

multiple input/output status buffers is available to store information about a completion of one or more pending input/output store instructions.

20. The computer-implemented method of claim 18, wherein the data processing unit comprises an asynchronous core-nest interface, the asynchronous core-nest interface comprising an input/output status array including the multiple input/output status buffers to collect returned states from the selected component, the selected component being a system nest communicatively coupled to the data processing unit via an aggregation buffer and to at least one external device, the aggregation buffer being further communicatively coupled to the asynchronous core-nest interface.